

## 7) Notes on power ON/OFF

- At power ON/OFF, set CS "L".

When CS is "H", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS "L". (When CS is in "L" status, all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS "L".

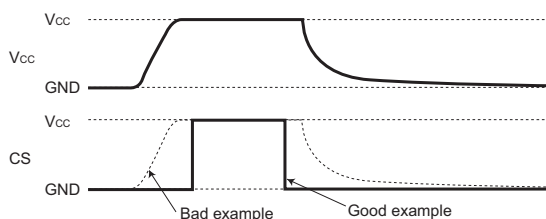


Fig. Timing at power ON/OFF

(Bad example) CS pin is pulled up to Vcc.

In this case, CS becomes "H" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes. Even when CS input is High-Z, the status becomes like this case, which please note.

(Good example) It is "L" at power ON/OFF.

Set 10ms or higher to recharge at power OFF. When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

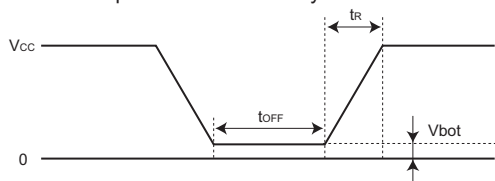
### ○POR circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.

After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may become write enable status owing to noises and the likes.

For secure actions, observe the following conditions.

- Set CS = "L".
- Turn on power so as to satisfy the recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$  for POR circuit action.



Recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$

$t_R$	$t_{OFF}$	$V_{bot}$
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Fig. Rise waveform diagram

### ○LVCC circuit

LVCC (Vcc - Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.

At LVCC voltage (Typ. = 1.2V) or below, it prevent data rewrite.