

● Write all area

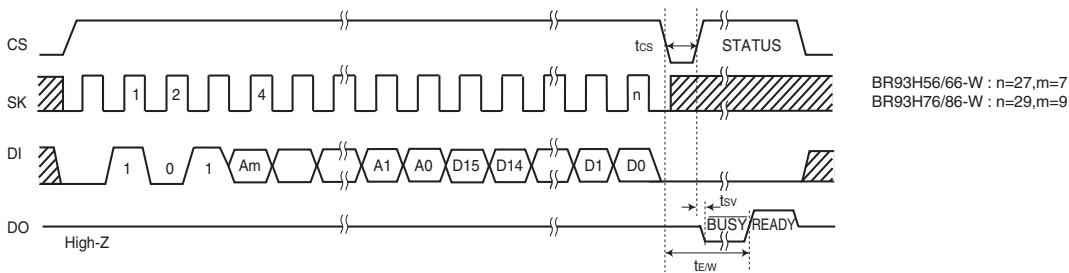
B2	B1	B0	Write area
0	0	0	000h ~ 07Fh
0	0	1	080h ~ 0FFh
0	1	0	100h ~ 17Fh
0	1	1	180h ~ 1FFh
1	0	0	200h ~ 27Fh
1	0	1	280h ~ 2FFh
1	1	0	300h ~ 37Fh
1	1	1	380h ~ 3FFh

Designation of B2, B1, and B0

H56	*	*	*
H66	*	*	B0
H76	*	B1	B0
H86	B2	B1	B0

- The write all command is written in bulk in 2Kbit unit.  
The write area can be selected up to 3bit. Confirm the settings and write areas of the above B2, B1, and B0.

● Write cycle (WRITE)



- In this command, input 16bit data (D15 ~ D0) are written to designated addresses (Am ~ A0). The actual write starts by the fall of CS from the rise of D0 taken SK clock (n-th clock from the start bit input), to the rise of the (n+1)-th clock.

When STATUS is not detected, (CS = "L" fixed) Max. 10ms in conformity with tE/W, and when STATUS is detected (CS = "H"), all commands are not accepted for areas where "L" ( $\overline{\text{BUSY}}$ ) is output from D0, therefore, do not input any command.

Write is not made even if CS is started after input of clock after (n+1)-th clocks.

Note ) Take tSKH or more from the rise of the n-th clock to the fall of CS.

Fig. Write cycle

● Write all cycle (WRAL)

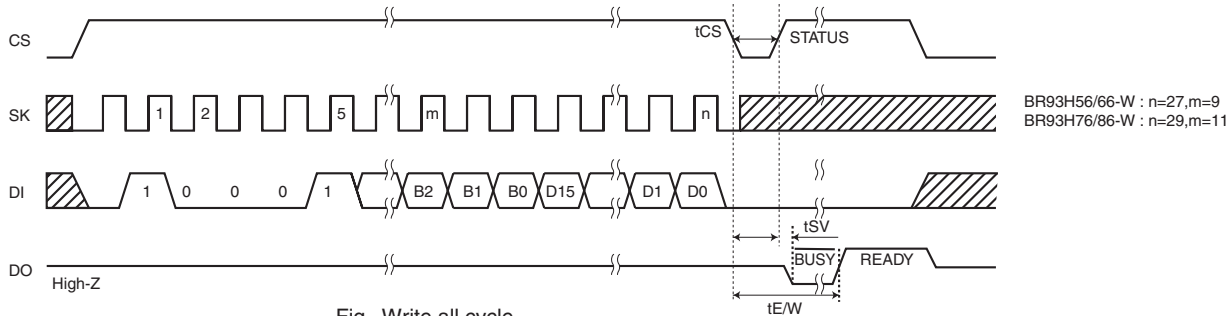


Fig. Write all cycle

- In this command, input 16bit data is written simultaneously to designated block for 128 words. Data is written in bulk at a write time of only Max. 10ms in conformity with tE/W. When writing data to all addresses, designate each block by B2, B1, and B0, and execute write. Write time is Max. 10ms. The actual write starts by the fall of CS from the rise of D0 taken at SK clock (n-th clock from the start bit input), to the rise of the (n+1)-th clock. When CS is ended after clock input after the rise of the (n+1)-th clock, command is cancelled, and write is not completed. Note: Take tSKH or more from the rise of the n-th clock to the fall of CS.

Designation of B2, B1, and B0

H56	*	*	*
H66	*	*	B0
H76	*	B1	B0
H86	B2	B1	B0