Power Management IC Series for Mobile Phone

High-efficiency Power Management ICs

BH6172GU

Structure	Silicon Monolithic Integrated Circuit
Product	Power Management LSI for MultiMedia LSI on Cellular
Type	**BH6172GU (Code name: VENUS)**
Package	Fig. 1
Block Diagram	Fig. 2
Application Circuit Example	Fig. 14~

Functions
- 1ch 500mA, high efficiency Step-down Converter. (16 steps adjustable VO by I^2C)
- 5-channel CMOS-type LDOs. (16 steps adjustable VO by I^2C, 150mA×3, 300mA×2)
- LDO and Stepdown converter Power ON/OFF control enabled by I2C interface or external pin
- I^2C compatible Interface. (Device address is “1001111”)
- Wafer Level CSP package(2.6mm×2.6mm) for space-constrained applications
- Discharge resistance selectable for power-down sequence ramp speed control

□This product is not especially designed to be protected from radioactivity.

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intended to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Sep. 2008

Absolute Maximum Ratings（Ta=25°C）

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage (VBAT)	VBATMAX	6.0	V
Maximum Supply Voltage (PBAT)	VPBATMAX	6.0	V
Maximum Supply Voltage (VUSB)	VUSBMAX	6.0	V
Maximum Input Voltage 1 (LX, FB, OUT1, OUT2, OUT3, OUT4, OUT5, EN_LD1, EN_LD2, EN_LD3, EN_LD4)	VINMAX1	VBAT + 0.3	V
Maximum Input Voltage 2 (NRST, CLK,DATA)	VINMAX2	DVDD + 0.3	V
Power Dissipation	Pd	900*[1]	mW
Operating Temperature Range	Topr	-35 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

* This is an allowable loss of the ROHM evaluation board(60mm×60mm).
When a substrate is implemented, the allowable loss varies from the size and material of the substrate.
To use at temperature higher than 25°C , derate 1% per 1°C.

Recommended Operating Conditions (Ta=25°C)

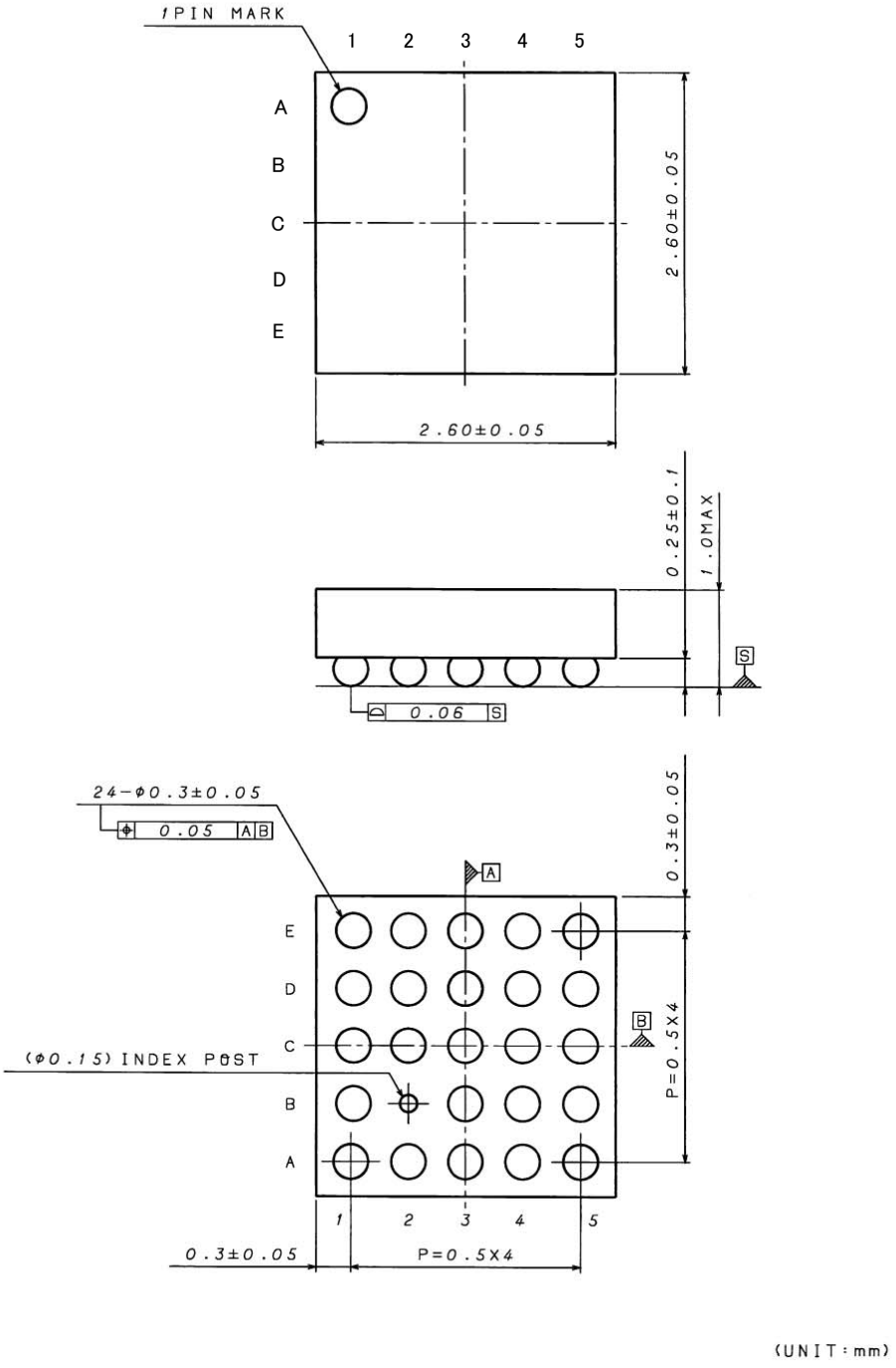
Parameter	Symbol	Range	Unit
VBAT Voltage	VBAT	*2 2.20 ～ 5.50	V
PBAT Voltage	VPBAT	*2 2.20 ～ 5.50	V
VUSB Voltage	VUSB	*2*3 2.20 ～ 5.50	V
DVDD Voltage	VDVDD	*4 1.70 ～ 4.20	V

*2 Whenever the VBAT or PBAT or VUSB voltage is under the LDO, SWREG output voltage, or else under certain levels, the LDO and SWREG output is not guaranteed to meet its published specifications.

*3 VUSB Power Supply can be externally connected to the VBAT, PBAT Power Supply when necessary.

*4 The DVDD Voltage must be under the Battery Voltage VBAT, PBAT at any times.

Package



(UNIT : mm)

Fig.1

Block diagram

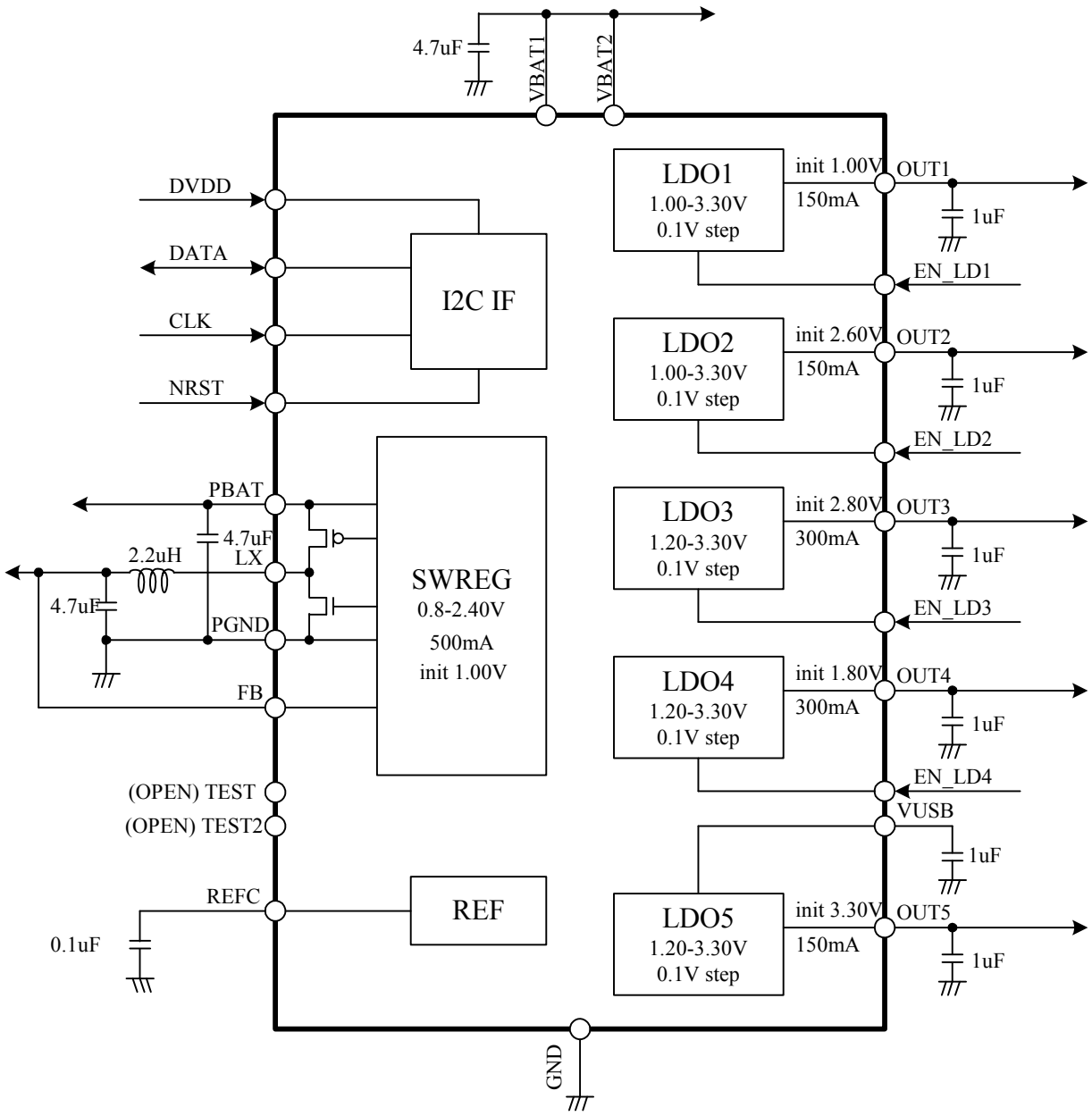


Fig.2

PIN description

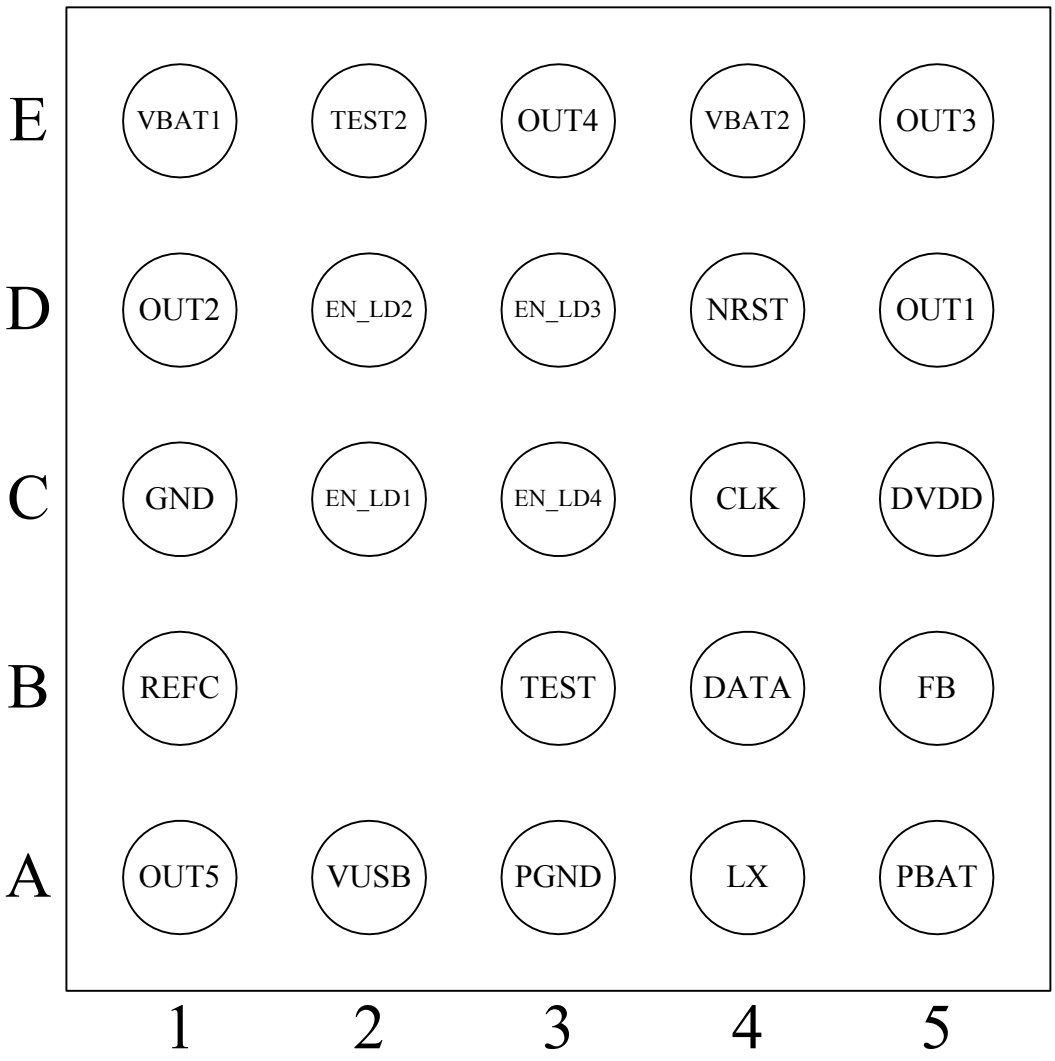


Fig.3

Ball No.	PIN Name	Function	ESD Diode	
			VBAT	GND
B4	DATA	Data input/output for I2c	O	O
C4	CLK	CLK input for I2c	O	O
E1	VBAT1	Power Supply 1	-	O
E4	VBAT2	Power Supply 2	-	O
A5	PBAT	Power Supply for SWREG	-	O
A4	LX	Inductor Connect pin 1 for SWREG	-	O
A3	PGND	Ground for SWREG	O	-
B5	FB	Voltage Feed back pin for SWREG	O	O
D4	NRST	RESET Input Pin (Low Active)	O	O
D5	OUT1	LDO1 Output	O	O
D1	OUT2	LDO2 Output	O	O
E5	OUT3	LDO3 Output	O	O
E3	OUT4	LDO4 Output	O	O
A1	OUT5	LDO5 Output	-	O
B1	REFC	Reference Voltage Output	-	O
C2	EN_LD1	LDO1 Enable Pin	O	O
D2	EN_LD2	LDO2 Enable Pin	O	O
D3	EN_LD3	LDO3 Enable Pin	O	O
C3	EN_LD4	LDO4 Enable Pin	O	O
A2	VUSB	*1 USBVBUS Power Supply	-	O
C5	DVDD	Digital Power Supply	-	O
C1	GND	Analog Ground	O	-
B3	TEST	TEST PIN (Always keep OPEN at normal use)	O	O
E2	TEST2	TEST PIN (Always keep OPEN at normal use)	O	O

* TEST, TEST2 pin is used during our company shipment test.
Please keep TEST pin and TEST2 pin "OPEN" at all times.

*1 VUSB Power Supply ball can be externally connected to the VBAT Power Supply when necessary.

(See Page 35~ for application examples)

	Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
SWREG	CORE	VBAT/PBAT	1.00V	500mA	0.80-2.40V
LDO1	CORE	VBAT	1.00V	150mA	1.00-3.30V
LDO 2	I/O1	VBAT	2.60V	150mA	1.00-3.30V
LDO3	MEMORY	VBAT	2.80V	300mA	1.20-3.30V
LDO 4	I/O2	VBAT	1.80V	300mA	1.20-3.30V
LDO5	USB	VBAT/VUSB	3.30V	150mA	1.20-3.30V

SWREG & LDOs Output Voltage table

	SWREG	LDO1	LDO2	LDO3	LDO4	LDO5
Programmable Output Voltages	0.80V	1.00V	1.00V	1.20V	1.20V	1.20V
	0.85V	1.10V	1.10V	1.30V	1.30V	1.30V
	0.90V	1.20V	1.20V	1.40V	1.40V	1.40V
	0.95V	1.30V	1.30V	1.50V	1.50V	1.50V
	1.00V	1.40V	1.40V	1.60V	1.60V	1.60V
	1.05V	1.50V	1.50V	1.70V	1.70V	1.70V
	1.10V	1.60V	1.60V	1.80V	1.80V	1.80V
	1.15V	1.70V	1.70V	1.85V	1.85V	1.85V
	1.20V	1.80V	1.80V	1.90V	1.90V	1.90V
	1.365V	1.85V	1.85V	2.00V	2.00V	2.00V
	1.40V	2.60V	2.60V	2.60V	2.60V	2.60V
	1.50V	2.70V	2.70V	2.70V	2.70V	2.70V
	1.65V	2.80V	2.80V	2.80V	2.80V	2.80V
	1.80V	2.85V	2.85V	2.85V	2.85V	2.85V
	1.85V	3.00V	3.00V	3.00V	3.00V	3.00V
	2.40V	3.30V	3.30V	3.30V	3.30V	3.30V

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●Circuit Current						
VBAT Circuit Current 1 (OFF)	IQVB1	-	0.4	1	μA	LDO1~5=OFF, SWREG1=OFF NRST=L DVDD=0V
VUSB Circuit Current 1 (OFF)	IQUSB1	-	0	1	μA	
VBAT Circuit Current 2 (OFF)	IQVB2	-	0.4	1	μA	LDO1~5=OFF, SWREG1=OFF NRST=L DVDD=0V VUSB=VBAT external connection
VBAT Circuit Current 3 (STANDBY)	IQVB3	-	0.7	1.4	μA	LDO1~5=OFF, SWREG1=OFF NRST=H DVDD=2.6V
VUSB Circuit Current 2 (STANDBY)	IQUSB2	-	0	1	μA	
VBAT Circuit Current 4 (STANDBY)	IQVB4	-	0.7	1.4	μA	LDO1~5=OFF, SWREG1=OFF NRST=H DVDD=2.6V VUSB=VBAT external connection

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

VBAT Circuit Current 5 (Active)	IQVB5	-	170	300	μA	LDO1~5=ON(no load, initial voltage) SWREG1=ON(no load, initial voltage) NRST=H DVDD=2.6V
VUSB Circuit Current 3 (Active)	IQUSB3	-	35	70	μA	
VBAT Circuit Current 6 (Active)	IQVB6	-	200	350	μA	LDO1~5=ON(no load, initial voltage) SWREG1=ON(no load, initial voltage) NRST=H DVDD=2.6V VUSB=VBAT external connection

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT=3.6V, VUSB=5.0V, DVDD=2.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
●Logic pin character							
NRST (CMOS input)	Input “H” level	VIH1	DVDD* 0.7	-	DVDD+ 0.3	V	Pin voltage: DVDD
	Input “L” level	VIL1	-0.3	-	DVDD* 0.3	V	Pin voltage: 0 V
	Input leak current	IIC1	0	0.3	1	μA	
EN_LD1, EN_LD2, EN_LD3, EN_LD4 (NMOS input)	Input “H” level	VIH2	1.44	-	-	V	
	Input “L” level	VIL2	-	-	0.4	V	
	Input leak current	IIC2	-1	0	1	μA	

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, VBAT=PBAT =3.6V, VUSB=5.0V, DVDD=2.6V)

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
●Digital characteristics (Digital pins: CLK and DATA)						
Input "H" level	VIH3	0.8× DVDD	-	DVDD+ 0.3	V	
Input "L" level	VIL3	-0.3	-	0.2× DVDD	V	
Input leak current	IIC3	-1	0	1	μA	Pin voltage: DVDD
DATA output "L" level voltage	VOL	-	-	0.4	V	IOL=6mA

Electrical Characteristics

AC Characteristics on I^2C bus.

Characteristics	Symbol	Min	Max	Unit
CLK clock frequency	f_{CLK}	0	400	kHz
CLK clock “low” time	t_{LOW}	1.3	-	μs
CLK clock “high” time	t_{HIGH}	0.6	-	μs
Bus free time	t_{BUF}	1.3	-	μs
Start condition hold time	$t_{HD.STA}$	0.6	-	μs
Start condition setup time	$t_{SU.STA}$	0.6	-	μs
Data input hold time	$t_{HD.DAT}$	0	-	ns
Data input setup time	$t_{SU.DAT}$	100	-	ns
Stop condition setup time	$t_{SU.STO}$	0.6	-	μs

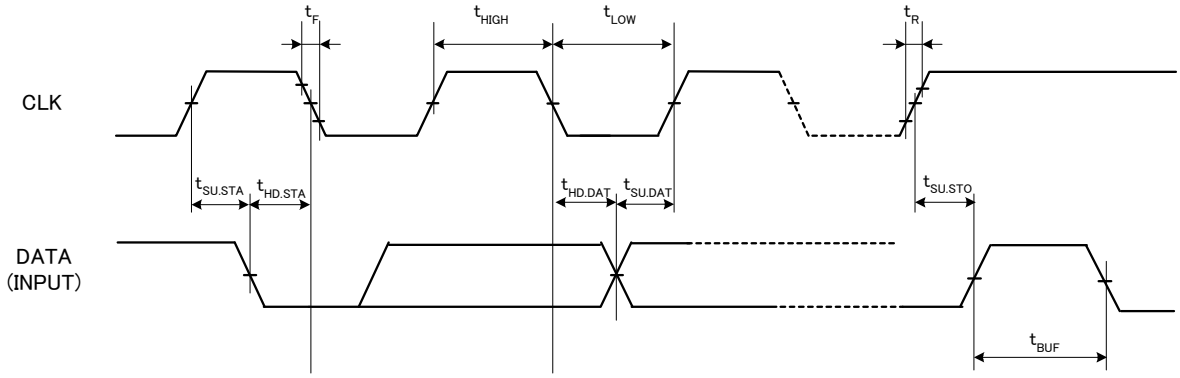


Figure 3 Bus Timing 1

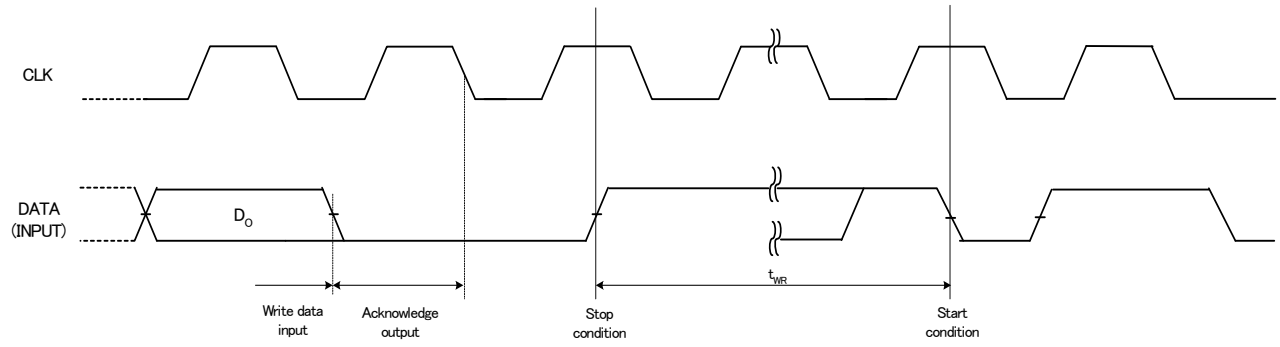


Figure 4 Bus Timing 2

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
●SWREG						
Output Voltage	VOSW	0.94	1.00	1.06	V	initial value Io=100mA
Programmable Output Voltage	VOSW10 VOSW11 VOSW12 VOSW13 VOSW14 VOSW15 VOSW16 VOSW17 VOSW18 VOSW19 VOSW1A VOSW1B VOSW1C VOSW1D VOSW1E VOSW1F	-	0.80 0.85 0.90 0.95 1.00 1.05 1.10 1.15 1.20 1.365 1.40 1.50 1.65 1.80 1.85 2.40	-	V	Io=100mA
Output current	IOSW	-	-	500	mA	Vo=1.00V
Efficiency	ηSW	-	90	-	%	Io=100mA, Vo=2.40V, VBAT=3.2V
Oscillating Frequency	f_{OSC}	-	1.7	-	MHz	Vo=1.00V
Output Inductance	L_{SWREG}	1.5	2.2	-	□H	Ta= -30～75°C
Output Capacitance	C_{SWREG}	3.3	4.7	-	□F	Ta= -30～75°C, with SWREG's DC bias

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●LDO1						
Output Voltage	VOM1	0.97	1.000	1.030	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output Current	VOM1C	-	-	150	mA	Vo=1.0V
Dropout Voltage	VOM1DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	⊿VIM1	-	2	-	mV	VBAT=3.4~4.5V, Io=50mA Vo=1.0V
Load Stability	⊿VLM1	-	20	-	mV	Io=50μA ~150mA, VBAT=3.6V Vo=1.0V
Programmable Output voltage	VOM10 VOM11 VOM12 VOM13 VOM14 VOM15 VOM16 VOM17 VOM18 VOM19 VOM1A VOM1B VOM1C VOM1D VOM1E VOM1F	-	1.00 1.10 1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.85 2.60 2.70 2.80 2.85 3.00 3.30	-	V	Io=50mA
Discharge Resistance1	R_{DCHG11}	-	1k	-	ohm	default ON
Discharge Resistance2	R_{DCHG12}	-	10k	-	ohm	default OFF
Ripple rejection ratio	RRM1	-	60	-	dB	VR=-20dBV fR=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Output Capacitor	COUT1	-	1.0	-	□F	Ta= -30～75°C, with LDO's DC bias

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●LDO2						
Output Voltage	VOM2	2.522	2.600	2.678	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output Current	VOM2C	-	-	150	mA	Vo=2.6V
Dropout Voltage	VOM2DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	⊿VIM2	-	2	-	mV	VBAT=3.4~4.5V, Io=50mA Vo=2.6V
Load Stability	⊿VLM2	-	20	-	mV	Io=50μA ~150mA, VBAT=3.6V Vo=2.6V
Programmable Output voltage	VOM20 VOM21 VOM22 VOM23 VOM24 VOM25 VOM26 VOM27 VOM28 VOM29 VOM2A VOM2B VOM2C VOM2D VOM2E VOM2F	-	1.00 1.10 1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.85 2.60 2.70 2.80 2.85 3.00 3.30	-	V	Io=50mA
Discharge Resistance1	R_{DCHG21}	-	1k	-	ohm	default ON
Discharge Resistance2	R_{DCHG22}	-	10k	-	ohm	default OFF
Ripple rejection ratio	RRM2	-	60	-	dB	VR=-20dBV fR=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Output Capacitor	COUT2	-	1.0	-	□F	Ta= -30～75°C, with LDO's DC bias

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●LDO3						
Output Voltage	VOM3	2.716	2.800	2.884	V	initial value Io=1mA@VBAT=4.5V Io=150mA@VBAT=3.4V
Output Current	VOM3C	-	-	300	mA	Vo=2.8V
Dropout Voltage	VOM3DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	⊿VIM3	-	2	-	mV	VBAT=3.4~4.5V, Io=50mA Vo=2.8V
Load Stability	⊿VLM3	-	20	-	mV	Io=50μA ~300mA, VBAT=3.6V Vo=2.8V
Programmable Output voltage	VOM30 VOM31 VOM32 VOM33 VOM34 VOM35 VOM36 VOM37 VOM38 VOM39 VOM3A VOM3B VOM3C VOM3D VOM3E VOM3F	-	1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.85 1.90 2.00 2.60 2.70 2.80 2.85 3.00 3.30	-	V	Io=50mA
Discharge Resistance1	R_{DCHG31}	-	1k	-	ohm	default ON
Discharge Resistance2	R_{DCHG32}	-	10k	-	ohm	default OFF
Ripple rejection ratio	RRM3	-	60	-	dB	VR=-20dBV fR=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Output Capacitor	COUT3	-	1.0	-	□F	Ta= -30～75°C, with LDO's DC bias

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●LDO4						
Output Voltage	VOM4	1.746	1.800	1.854	V	initial value Io=1mA@VBAT=4.5V Io=300mA@VBAT=3.4V
Output Current	VOM4C	-	-	300	mA	Vo=1.8V
Dropout Voltage	VOM4DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	⊿VIM4	-	2	-	mV	VBAT=3.4~4.5V, Io=50mA Vo=1.8V
Load Stability	⊿VLM4	-	30	-	mV	Io=50μA ~300mA, VBAT=3.6V Vo=1.8V
Programmable Output voltage	VOM40 VOM41 VOM42 VOM43 VOM44 VOM45 VOM46 VOM47 VOM48 VOM49 VOM4A VOM4B VOM4C VOM4D VOM4E VOM4F	-	1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.85 1.90 2.00 2.60 2.70 2.80 2.85 3.00 3.30	-	V	Io=50mA
Discharge Resistance1	R_{DCHG41}	-	1k	-	ohm	default ON
Discharge Resistance2	R_{DCHG42}	-	10k	-	ohm	default OFF
Ripple rejection ratio	RRM4	-	60	-	dB	VR=-20dBV fR=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Output Capacitor	COUT4	-	1.0	-	□F	Ta= -30～75°C, with LDO's DC bias

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PBAT =3.6V, VUSB=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●LDO5						
Output Voltage	VOM5	3.201	3.300	3.399	V	initial value Io=1mA@VUSB=5.5V Io=150mA@VUSB=4.4V
Output Current	VOM5C	-	-	150	mA	Vo=3.3V
Dropout Voltage	VOM5DP	-	0.1	-	V	Io=50mA
Input Voltage Stability	⊿VIM5	-	2	-	mV	VUSB=4.4~5.5V, Io=50mA Vo=3.3V
Load Stability	⊿VLM5	-	20	-	mV	Io=50μA ~150mA, VUSB=5.5V Vo=3.3V
Programmable Output voltage	VOM50 VOM51 VOM52 VOM53 VOM54 VOM55 VOM56 VOM57 VOM58 VOM59 VOM5A VOM5B VOM5C VOM5D VOM5E VOM5F	-	1.20 1.30 1.40 1.50 1.60 1.70 1.80 1.85 1.90 2.00 2.60 2.70 2.80 2.85 3.00 3.30	-	V	Io=50mA
Discharge Resistance1	R_{DCHG51}	-	1k	-	ohm	default ON
Discharge Resistance2	R_{DCHG52}	-	10k	-	ohm	default OFF
Ripple rejection ratio	RRM5	-	60	-	dB	VR=-20dBV fR=120Hz Io=50mA, Vo=2.6V BW=20Hz～20kHz
Output Capacitor	COUT5	-	1.0	-	□F	Ta= -30～75°C, with LDO's DC bias

I^2C Bus INTERFACE

The I2C compatible synchronous serial interface provides access to programmable functions and register on the device.
This protocol uses a two-wire interface for bi-directional communications between the LSI's connected to the bus.
The two interface lines are the Serial Data Line(DATA), and the Serial Clock Line(CLK). These lines should be connected to the power supply DVDD by a pull-up resistor, and remain high even when the bus is idle.

1. Start and Stop Conditions

When CLK is high, pulling DATA low produces a start condition and pulling DATA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition occurs.

During read, a stop condition causes the read to terminate and the chip enters the standby state. During write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. Upon the completion of writing, the chip enters the standby state.

Two or more start conditions cannot be entered consecutively.

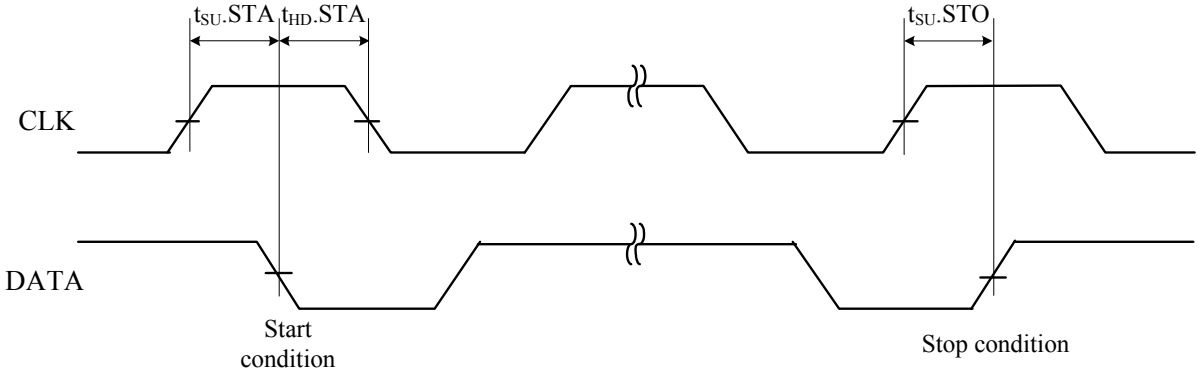


Figure 5

2. Modifying Data

Data on the DATA input can be modified while CLK is low. When CLK is high, modifying the DATA input means a start or stop condition.

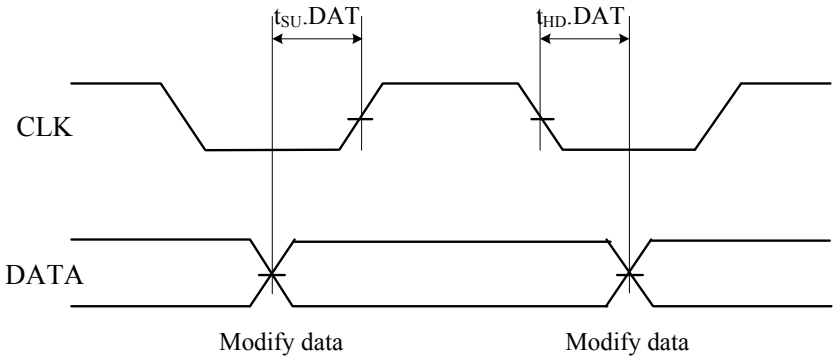


Figure 6

3. Acknowledge

Data is transmitted and received in 8-bit units. The receiver sends an acknowledge signal by outputting a low on DATA in the 9th clock cycle, indicating that it has received data normally. The transmitter releases the bus in the 9th clock cycle to receive an acknowledge signal.

During write, the chip is always the receiver so that it outputs an acknowledge signal each time it has received eight bits of data.

During read, the chip outputs an acknowledge signal after it receives an address following a start condition. Then, it outputs read data and releases the bus to wait for an acknowledge signal from the master. When it detects an acknowledge signal, it outputs data at the next address if it does not detect a stop condition. If the chip does not detect an acknowledge signal, it stops read operation, and enters the standby state when a stop condition occurs subsequently.

If the chip does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

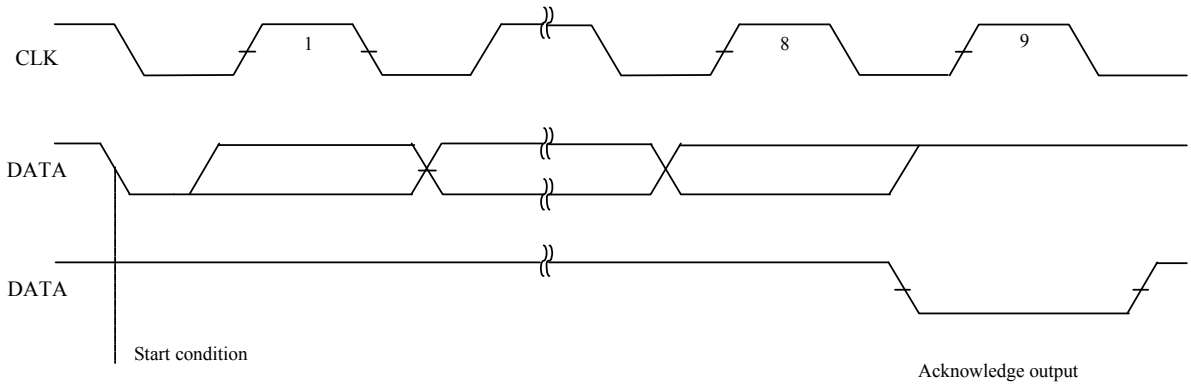


Figure 7

4. Device Addressing

After a start condition occurs, a 7-bit device address and a 1-bit read/write instruction code are inputted into the chip.

The upper seven bits are called device address, which must always be " 1001111".

The least significant bit *(R/W : READ/WRITE)* indicates a read instruction when set to 1 and a write instruction when set to 0.

An instruction is not executed if the device address does not match the specified value.

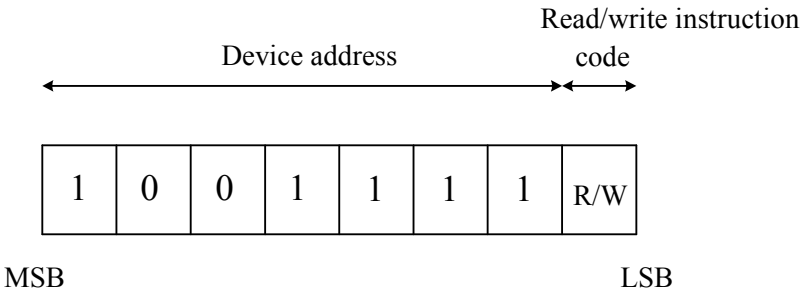


Figure 8

Device address is " 1001111".

5. Write operation

In order to write a specified address, after a start condition, input a device address, $R/W(=0)$, a word address, and write data.

When a stop condition is entered, the chip automatically enters standby state.

Address increment is acknowledged only whenever INC bit is'0'.

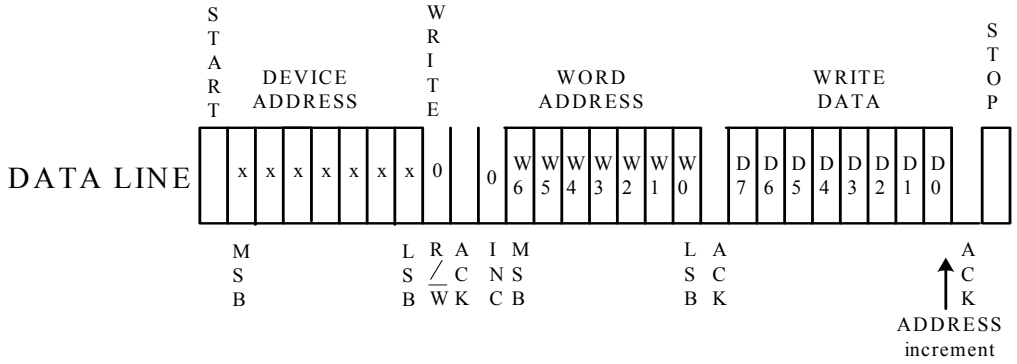


Figure 9

<Address increment ON>

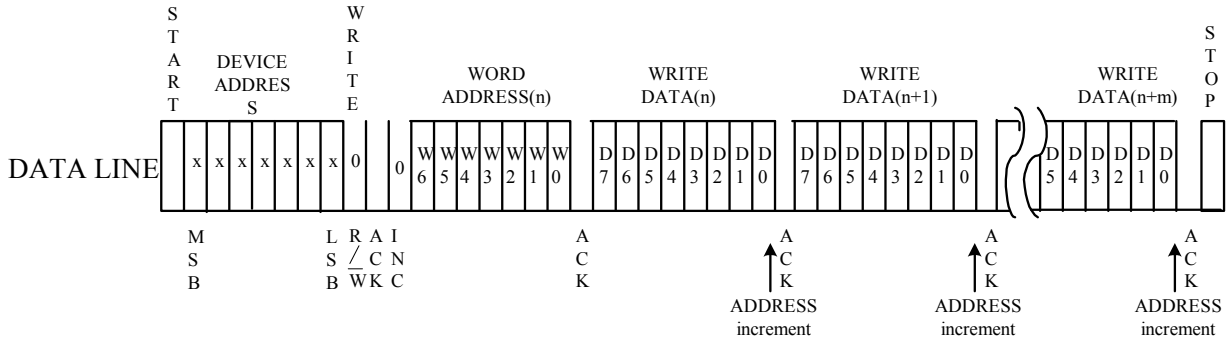


Figure 10

<Address increment OFF>

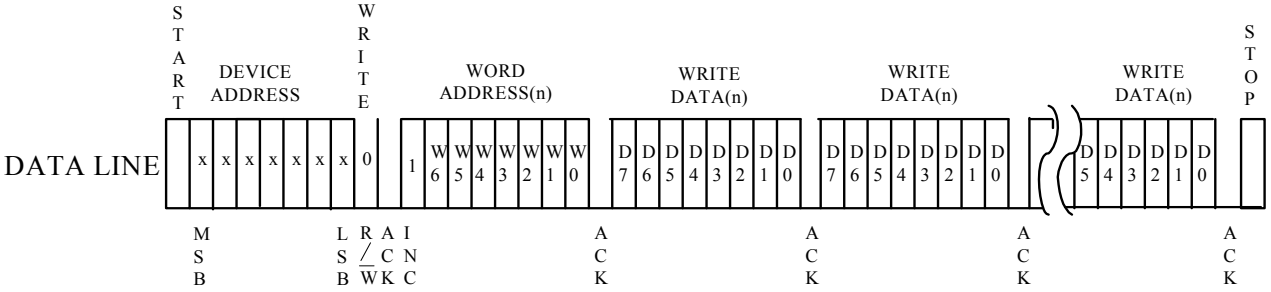


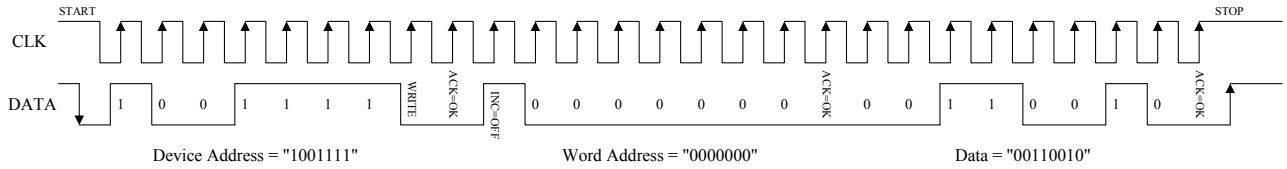
Figure 11

Roll over function operates when address increment is ON, after a start condition, input a device address, $R/W(=0)$, a word address (n), and write data (n), in the same way as for a byte write. Then, input write data $(n+1)$ immediately without entering a stop condition, while checking that an acknowledge signal is asserted (0).

When the last address (07H) is reached, the word address is rolled over to the first address (00H) of the page.

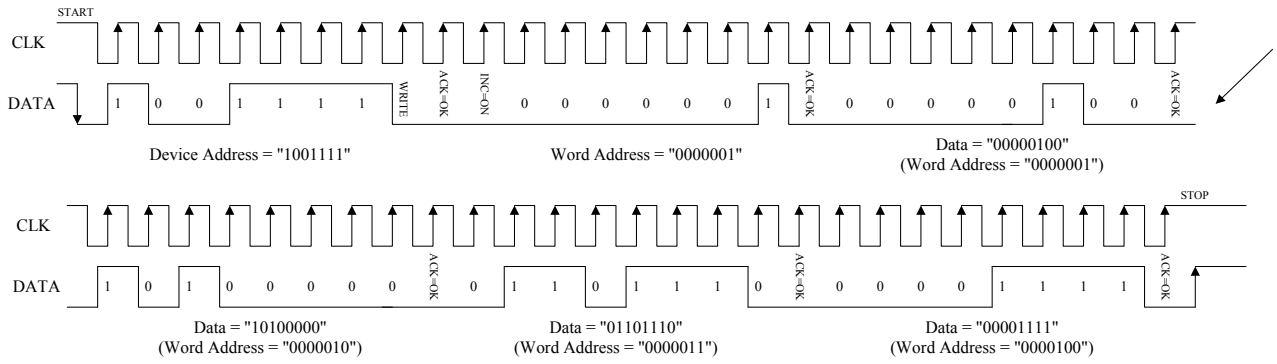
Write operation example (Auto Increment OFF)

(Write to Address 00h, Data 32h)
When writing to a single address follow the sequence below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => DATA => STOP
At this time, the Auto increment bit (=INC) can be either ‘H’ or ‘L’.



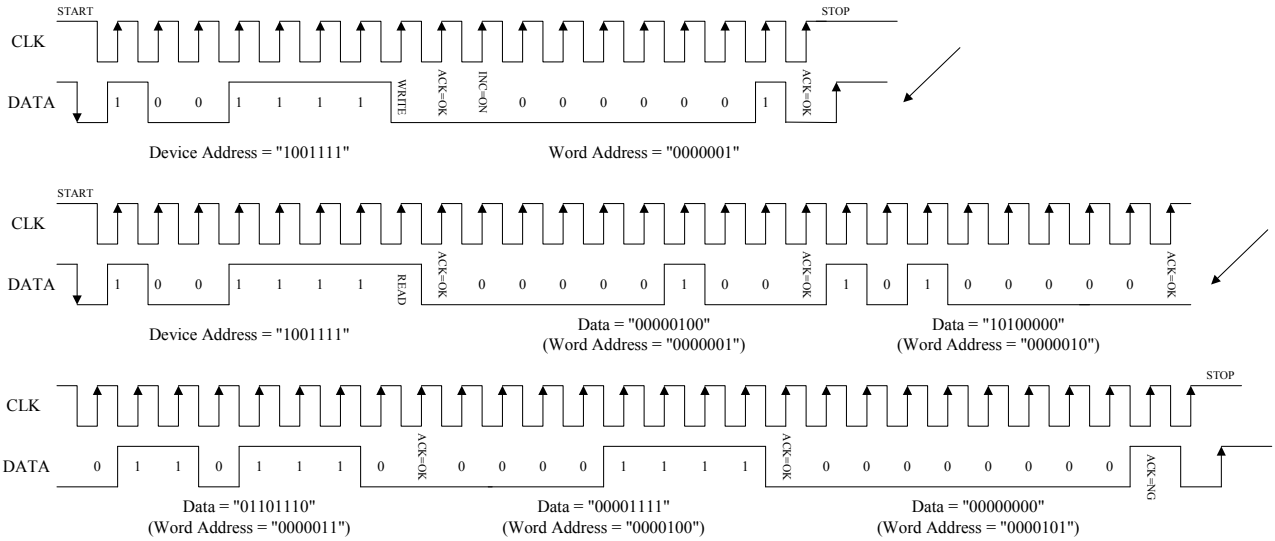
Write operation example (Auto Increment ON)

(Write to Address 01h, Data 04h;
Address 02h, Data A0h;
Address 03h, Data 6Eh;
Address 04h, Data 0Fh)
When writing to multiple addresses follow the sequence below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => DATA => DATA => DATA => DATA => STOP
At this time, the Auto increment bit (=INC) needs to be ‘L’.
When writing the Word address, write the first address which you want to start writing from.



Read operation example (Auto Increment ON)

(Read from Address 01h, 02h, 03h, 04h, 05h)
To read from Address 01h, you must first dummy write to Address 01h.
At this time, the Auto increment bit (=INC) needs to be ‘L’.
When finish reading, you must end by returning an ACK=NG(‘H’), and then stop.
The read sequence would be as shown below.
START => DEVICE ADDRESS+WRITE => WORD ADDRESS => STOP => START => DEVICE ADDRESS+READ =>
DATA READ + ACK OK => DATA READ + ACK OK => DATA READ + ACK OK => DATA READ + ACK OK => DATA READ + ACK NG => STOP



Register map

Address	Register name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0
00h	REGCNT	R/W	00h	-	-	LDO5ON	LDO4ON	LDO3ON	LDO2ON	LDO1ON	SWREGON
01h	SWADJ	R/W	04h	-	-	-	-	SWREGADJ [3:0]			
02h	LDOADJ1	R/W	A0h	LDO2ADJ [3:0]				LDO1ADJ [3:0]			
03h	LDOADJ2	R/W	6Eh	LDO4ADJ [3:0]				LDO3ADJ [3:0]			
04h	LDOADJ3	R/W	0Fh	-	-	-	-	LDO5ADJ [3:0]			
05h	PDSEL	R/W	00h	-	-	LDO5PD SEL	LDO4PD SEL	LDO3PD SEL	LDO2PD SEL	LDO1PD SEL	SWPD SEL
06h	PDCNT	R/W	3Fh	-	-	LDO5PD	LDO4PD	LDO3PD	LDO2PD	LDO1PD	SWPD
07h	EN_SEL	R/W	00h	-	-	-	-	ENLD4_EN	ENLD3_EN	ENLD2_EN	ENLD1_EN

The reset of the address 00h to 07h is the logic pin NRST.

* Please be sure to write “0” to the register which is not used(00h~07h).
* Writing to the address which is not assigned is prohibited.(08h~7Fh)
* Reading the data which address is not used is “0”.(00h~07h)
* Reading the data which address is not assigned is not guaranteed to be “0”.(08h~7Fh)

Address 00h : REGCNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	REGCNT	R/W	-	-	LDO5ON	LDO4ON	LDO3ON	LDO2ON	LDO1ON	SWREGON
Initial Value		00h	0	0	0	0	0	0	0	0

Bit0: SWREGON SWREG Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Bit1: LDO1ON LDO1 Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Bit2: LDO2ON LDO2 Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Bit3: LDO3ON LDO3 Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Bit4: LDO4ON LDO4 Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Bit5: LDO5ON LDO5 Power ON/OFF control
"0" : OFF (Initial State)
"1" : ON

Address 01h : SWADJ Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	SWADJ	R/W	-	-	-	-	SWREGADJ [3:0]			
Initial Value		04h	0	0	0	0	0	1	0	0

Bit [3:0]: SWREGADJ[3:0] SWREG Stepdown Converter output voltage control

"0000" : 0.80V
"0001" : 0.85V
"0010" : 0.90V
"0011" : 0.95V
"0100" : 1.00V (Initial State)
"0101" : 1.05V
"0110" : 1.10V
"0111" : 1.15V
"1000" : 1.20V
"1001" : 1.365V
"1010" : 1.40V
"1011" : 1.50V
"1100" : 1.65V
"1101" : 1.80V
"1110" : 1.85V
"1111" : 2.40V

Address 02h : LDOADJ1 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	LDOADJ1	R/W	LDO2ADJ [3:0]				LDO1ADJ [3:0]			
Initial Value		A0h	1	0	1	0	0	0	0	0

Bit [3:0]: LDO1ADJ [3:0] LDO1 output voltage control

"0000" : 1.00V (Initial State)
"0001" : 1.10V
"0010" : 1.20V
"0011" : 1.30V
"0100" : 1.40V
"0101" : 1.50V
"0110" : 1.60V
"0111" : 1.70V
"1000" : 1.80V
"1001" : 1.85V
"1010" : 2.60V
"1011" : 2.70V
"1100" : 2.80V
"1101" : 2.85V
"1110" : 3.00V
"1111" : 3.30V

Bit [7:4]: LDO2ADJ [3:0] LDO2 output voltage control

"0000" : 1.00V
"0001" : 1.10V
"0010" : 1.20V
"0011" : 1.30V
"0100" : 1.40V
"0101" : 1.50V
"0110" : 1.60V
"0111" : 1.70V
"1000" : 1.80V
"1001" : 1.85V
"1010" : 2.60V (Initial State)
"1011" : 2.70V
"1100" : 2.80V
"1101" : 2.85V
"1110" : 3.00V
"1111" : 3.30V

Address 03h : LDOADJ2 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	LDOADJ2	R/W	LDO4ADJ [3:0]				LDO3ADJ [3:0]			
Initial Value		6Eh	0	1	1	0	1	1	1	0

Bit [3:0]: LDO3ADJ [3:0] LDO3 output voltage control

"0000" : 1.20V
"0001" : 1.30V
"0010" : 1.40V
"0011" : 1.50V
"0100" : 1.60V
"0101" : 1.70V
"0110" : 1.80V
"0111" : 1.85V
"1000" : 1.90V
"1001" : 2.00V
"1010" : 2.60V
"1011" : 2.70V
"1100" : 3.00V
"1101" : 2.85V
"1110" : 2.80V (Initial State)
"1111" : 3.30V

Bit [7:4]: LDO4ADJ [3:0] LDO4 output voltage control

"0000" : 1.20V
"0001" : 1.30V
"0010" : 1.40V
"0011" : 1.50V
"0100" : 1.60V
"0101" : 1.70V
"0110" : 1.80V (Initial State)
"0111" : 1.85V
"1000" : 1.90V
"1001" : 2.00V
"1010" : 2.60V
"1011" : 2.70V
"1100" : 2.80V
"1101" : 2.85V
"1110" : 3.00V
"1111" : 3.30V

Address 04h : LDOADJ3 Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	LDOADJ3	R/W	-	-	-	-	LDO5ADJ [3:0]			
Initial Value		0Fh	0	0	0	0	1	1	1	1

Bit [3:0]: LDO5ADJ [3:0] LDO5 output voltage control

"0000" : 1.20V
"0001" : 1.30V
"0010" : 1.40V
"0011" : 1.50V
"0100" : 1.60V
"0101" : 1.70V
"0110" : 1.80V
"0111" : 1.85V
"1000" : 1.90V
"1001" : 2.00V
"1010" : 2.60V
"1011" : 2.70V
"1100" : 2.80V
"1101" : 2.85V
"1110" : 3.00V
"1111" : 3.30V (Initial State)

Address 05h : PDSEL Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	PDSEL	R/W	-	-	LDO5PDSEL	LDO4PDSEL	LDO3PDSEL	LDO2PDSEL	LDO1PDSEL	SWPDSEL
Initial Value		00h	0	0	0	0	0	0	0	0

Bit [0]: SWPDSEL SWREG pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Bit [1]: LDO1PDSEL LDO1 pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Bit [2]: LDO2PDSEL LDO2 pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Bit [3]: LDO3PDSEL LDO3 pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Bit [4]: LDO4PDSEL LDO4 pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Bit [5]: LDO5PDSEL LDO5 pulldown impedance select
"0" : 1k ohm (Initial State)
"1" : 10k ohm

Address 06h : PDCNT Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	PDCNT	R/W	-	-	LDO5PD	LDO4PD	LDO3PD	LDO2PD	LDO1PD	SWPD
Initial Value		3Fh	0	0	1	1	1	1	1	1

Bit [0]: SWPD SWREG Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Bit [1]: LDO1PD LDO1 Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Bit [2]: LDO2PD LDO2 Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Bit [3]: LDO3PD LDO3 Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Bit [4]: LDO4PD LDO4 Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Bit [5]: LDO5PD LDO5 Output impedance control during power_off
"0" : Hi-Z
"1" : Discharge enabled (Initial State)

Address 07h : EN_SEL Register (Read/Write)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	EN_SEL	R/W	-	-	-	-	ENLD4_EN	ENLD3_EN	ENLD2_EN	ENLD1_EN
Initial Value		00h	0	0	0	0	0	0	0	0

Bit [0]: ENLD1_EN LDO1 ON/OFF Control select
"0" : LDO1 ON/OFF control by EN_LD1 pin (Initial State)
"1" : LDO1 ON/OFF control by LDO1ON register

Bit [1]: ENLD2_EN LDO2 ON/OFF Control select
"0" : LDO2 ON/OFF control by EN_LD2 pin (Initial State)
"1" : LDO2 ON/OFF control by LDO2ON register

Bit [2]: ENLD3_EN LDO3 ON/OFF Control select
"0" : LDO3 ON/OFF control by EN_LD3 pin (Initial State)
"1" : LDO3 ON/OFF control by LDO3ON register

Bit [3]: ENLD4_EN LDO4 ON/OFF Control select
"0" : LDO4 ON/OFF control by EN_LD4 pin (Initial State)
"1" : LDO4 ON/OFF control by LDO4ON register

6. Notes on Use

a) Pulling up the DATA and CLK pins

This IC requires the DATA and CLK pins to be pulled up with an external resistor. The values of the pull-up resistors are determined by the capacitance of the bus. Too large of a resistor combined with a given bus capacitance will result in a rise time that would violate the max rise time specification. A too small resistor will result in a contention with the pull-down transistor on either slave or master. The recommended pull-up resistance range is 1kohm to 10kohm.

To decide the value of the pull-up resistance, you can calculate by using the equation R=t/C.

t : DATA, CLK rise time to meet the I2C AC specification.

C : Total Bus capacitance on each DATA, CLK lines.

For example, to meet the specification 100ns rise time, 100pF total bus capacitance, the desired resistance is

R=100ns/100pF = 1kohm.

b) Enable Pins(EN_LD1~EN_LD4)

Applying a voltage of 0.4V or less at the Enable pin will disable the output, reducing the quiescent output current to less than 1uA, while a voltage of 1.44V or greater will enable the device. (When Enable pins are selected as ON/OFF control.)

If any of the Enable pins are not used in the system, the pins can simply be connected to the GND pin. Allowing these pins to float will cause erratic operation.

7. PCB Layout Recommendations

Good PCB layout plays an important role especially in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedbacks that can affect the performance of the converter.

Hints suggested below can be used as a guideline in most situations.

a) Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path.

b) Components Placement

Power components, i.e. input capacitor, inductor and outside capacitor, must be placed close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (FB, ball B5) terminal to avoid unwanted injection of noise into the feedback path.

c) Feedback Path

Feedback of the output voltage must be a separate trace separated from the power path. The output voltage sensing trace to the feedback (FB, ball B5) terminal should be connected to the output voltage directly at the anode of the output capacitor.

Power ON/OFF control 1 （EN_LD* pin boot→Off Sequence by EN_LD* pin）

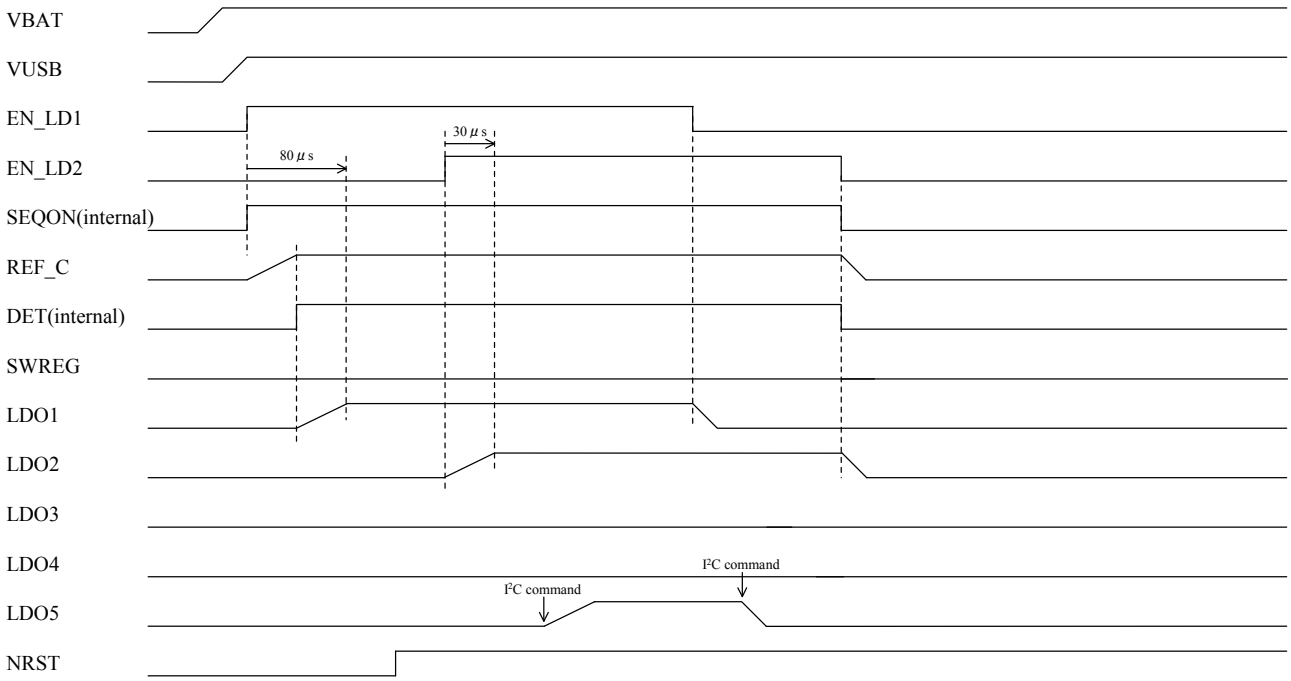


Figure 12

Whenever all LDO's and SWREG is all OFF, the internal SEQON signal is always 'L'. At that time, the device is in either OFF or in STANDBY mode, so the quiescent current is under 1uA. The first LDO to bootup takes time depending on the time the reference voltage REF_C comes up. The time showed above is not guaranteed, and will change for example by load conditions.
The device can be booted up by either the EN_LD1~EN_LD4 pins or by I2C register control.
When the device is booted up by the EN_LD1~EN_LD4 pins, NRST and DVDD power supply can be at any level.
Operation of the BH6172GU without the I2C interface is possible if the system can operate with default values for the LDO1~4.
The I2C-less system must rely on the correct default output values of the LDO1~4. Whenever the LDO and SWREG output voltages need changes from the default output values, access from the I2C interface is always necessary.
SWREG and LDO5 can only be activated by the I2C interface because there is no external enable pin for these channels.

LDO5 is designed to supply the 3.3V for USB peripherals. The power source for LDO5 is VUSB, therefore whenever turning LDO5=ON, VUSB power supply is required.
It is recommended for VUSB to be connected to the 5V VBUS power supply individually for best results. But it can be connected to the VBAT power supply if LDO5 is not intended to be used for the 3.3V USB supply. When VUSB is connected to VBAT, LDO5 may not be possible to maintain the 3.3V supply to the USB peripherals when VBAT voltage is at a low level. Whenever using LDO5 as USB 3.3V supply, always connect the VUSB terminal to 5V VBUS power supply at all times.
If LDO5 is to be used as an optional LDO as LDO1~4, connect VUSB to VBAT power source externally.

Power ON/OFF control 2 （I2C register boot→Off Sequence by I2C register）

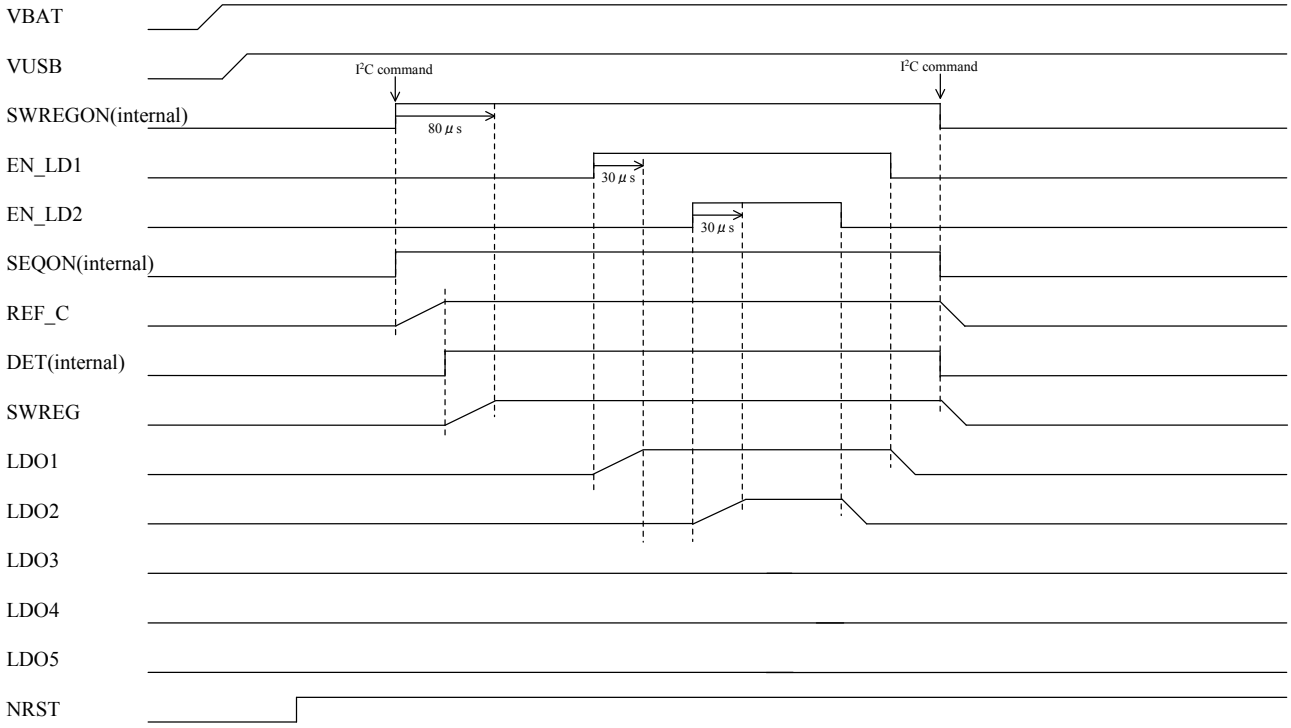


Figure 13

This device can also be activated by the I2C register as shown above. The time to bootup is similar to that of Power ON/OFF control 1.
When the device is booted up by the I2C registers, DVDD power supply is needed for the I2C logic to operate, and NRST must be forced ‘H’ for the I2C interface to be enabled.
LDO1~4 is controlled by EN_LD1~4 pins by default, but can be changed to I2C register control at any time.
LDO5, SWREG is controllable only by the I2C register.
There is no ON/OFF sequence equipped in this device. Any ON/OFF sequence can be performed freely by external control.

BH6172GU Application Circuit Example

There are mainly 3 ways to operate BH6172GU.

1. Fully I2C operation
2. I2C-free operation
3. Enable Pin & I2C interface hybrid operation

1-1(a) Fully I2C operation

When EN_LD1~4 pins are not used, connect all pins to GND level.

All SWREG, LDO channels can be freely turned ON/OFF by the corresponding I2C registers.

Any boot sequence can be performed by the I2C registers.

The output voltages can be changed freely on all LDO1~5, and also SWREG.

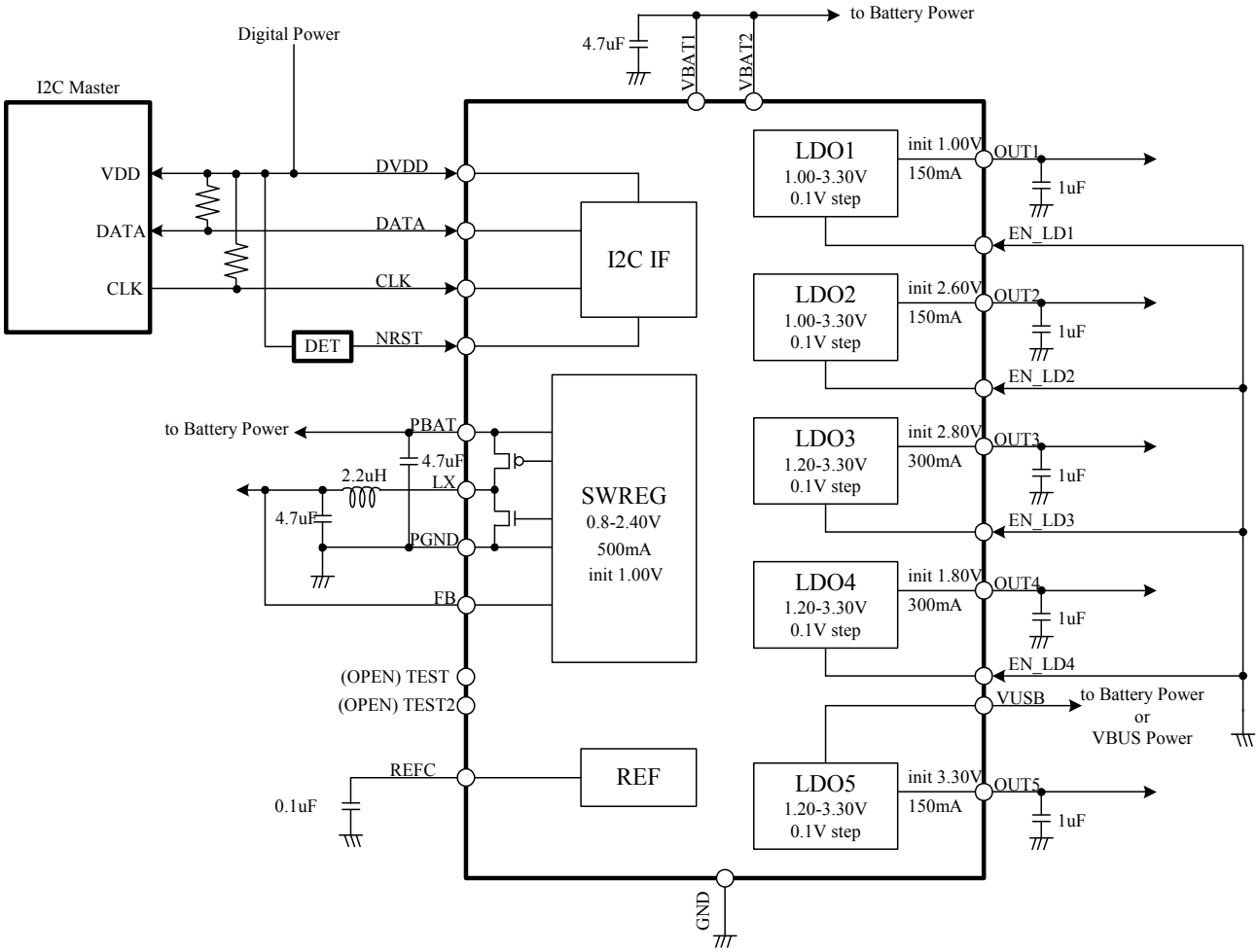


Figure 14 Application example for Fully-I2C operation mode

1-1(b) Boot sequence example 1
<Condition Sample>
Output Voltage : SWREG=1.20V
: LDO1=1.00V
: LDO2=OFF
: LDO3=2.60V
: LDO4=1.80V
: LDO5=2.80V
On Sequence : LDO1, 3, 4 -> SWREG -> LDO5
Off Sequence : LDO5 -> SWREG -> LDO1, 3, 4
SWREG, LDO1~5=1kohm discharge select
SWREG, LDO1~5=All discharge enabled
EN_LD1~4 enable pins disabled, LDO1~4 controlled by I2C control

<On Sequence Sample>
VBAT, VUSB, PBAT=Power Supply ON
DVDD=Power Supply ON
NRST=L -> H force
I2C: Address=01h, Data=08h : SWREG=1.20V setting
I2C: Address=02h, Data=A0h : LDO1=1.00V, LDO2=2.60V setting
I2C: Address=03h, Data=6Ah : LDO3=2.60V, LDO4=1.80V setting
I2C: Address=04h, Data=0Ch : LDO5=2.80V setting
I2C: Address=05h, Data=00h : SWREG, LDO1~5=1kohm discharge setting
I2C: Address=06h, Data=3Fh : SWREG, LDO1~5=All discharge enabled
I2C: Address=07h, Data=0Fh : LDO1~4=ON/OFF control performed by I2C register

I2C: Address=00h, Data=40h : BGR=ON(This command is highly recommended to maintain boot stability)
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=1Ah : LDO1, 3, 4=ON
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=1Bh : SWREG=ON
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=3Bh : LDO5=ON
~~~~~~
<Off Sequence Sample>
□I2C: Address=00h, Data=1Bh : LDO5=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=1Ah : SWREG=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=00h : LDO1, 3, 4=OFF
~~~~~~

Power ON/OFF sample 1（Fully I2C operation)

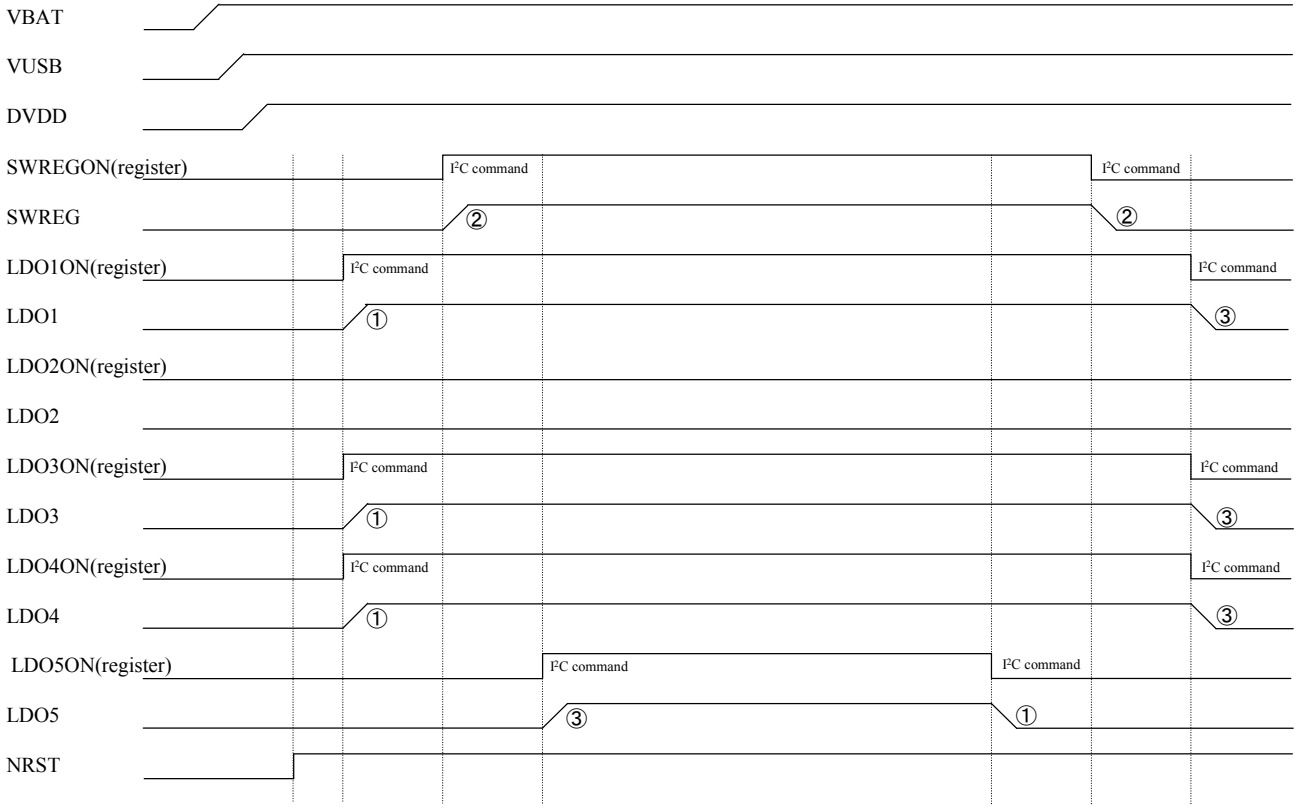


Figure 15　I2C full control ON/OFF waveform example 1

When all SWREG, and LDO's are only controllable by I2C, the minimum timing interval is approximately 23us which is dependant on the I2C CLK frequency.
As it is capable of booting up all SWREG, LDO1~5 all at the same time, it is likely in most situations that a huge rush current will flow through each power supply. Care should be taken such as to maintain certain appropriate timing intervals between each LDO or SWREG during the boot-up sequence to avoid any unwanted drops in VBAT power supplies which may cause total system failure.

1-2(a) Boot sequence example 2
<Condition Sample>
Output Voltage : SWREG=1.20V
: LDO1=1.00V
: LDO2=2.60V
: LDO3=2.60V
: LDO4=1.80V
: LDO5=2.80V
On Sequence : LDO1, 2, 3, 4, 5, SWREG all at the same time
Off Sequence : LDO1, 2, 3, 4, 5, SWREG all at the same time
SWREG, LDO1~5=1kohm discharge select
SWREG, LDO1~5=All discharge enabled
EN_LD1~4 enable pins disabled, LDO1~4 controlled by I2C control

<On Sequence Sample>
VBAT, VUSB, PBAT=Power Supply ON
DVDD=Power Supply ON
NRST=L -> H force
I2C: Address=01h, Data=08h : SWREG=1.20V setting
I2C: Address=02h, Data=A0h : LDO1=1.00V, LDO2=2.60V setting
I2C: Address=03h, Data=6Ah : LDO3=2.60V, LDO4=1.80V setting
I2C: Address=04h, Data=0Ch : LDO5=2.80V setting
I2C: Address=05h, Data=00h : SWREG, LDO1~5=1kohm discharge setting
I2C: Address=06h, Data=3Fh : SWREG, LDO1~5=All discharge enabled
I2C: Address=07h, Data=0Fh : LDO1~4=ON/OFF control performed by I2C register

I2C: Address=00h, Data=40h : BGR=ON(This command is highly recommended to maintain boot stability)
Interval time inserted (for example 1ms, minimum 0ms)
I2C: Address=00h, Data=3Fh : LDO1, 2, 3, 4, 5, SWREG=ON
~~~~~~
<Off Sequence Sample>
I2C: Address=00h, Data=00h : LDO1, 2, 3, 4, 5, SWREG=OFF
~~~~~~

Power ON/OFF sample 2（Fully I2C operation)

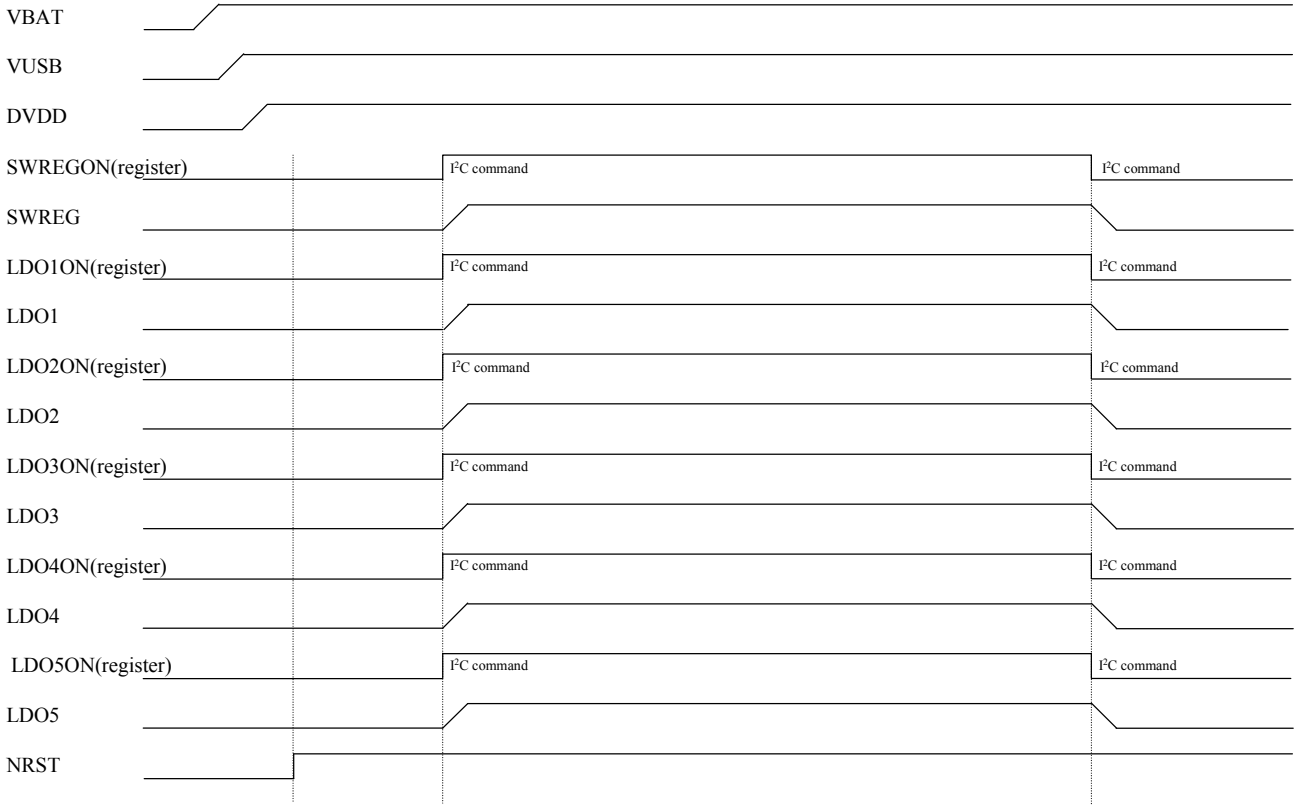


Figure 16　I2C full control ON/OFF waveform example 2

When booting up all SWREG, LDO1~5 all at the same time, it is likely in most situations that a huge rush current will flow through each power supply. Care should be taken in monitoring any drops in VBAT power supply which may cause total system failure.

2-1(a) I2C-free mode

LDO1~4 can be freely turned ON/OFF by the corresponding enable pins EN_LD1~4.

Any boot sequence can be performed by the external Application CPU etc.

Since the output voltages can be changed only by the I2C interface, LDO1~4 can only be used by the initial voltages.

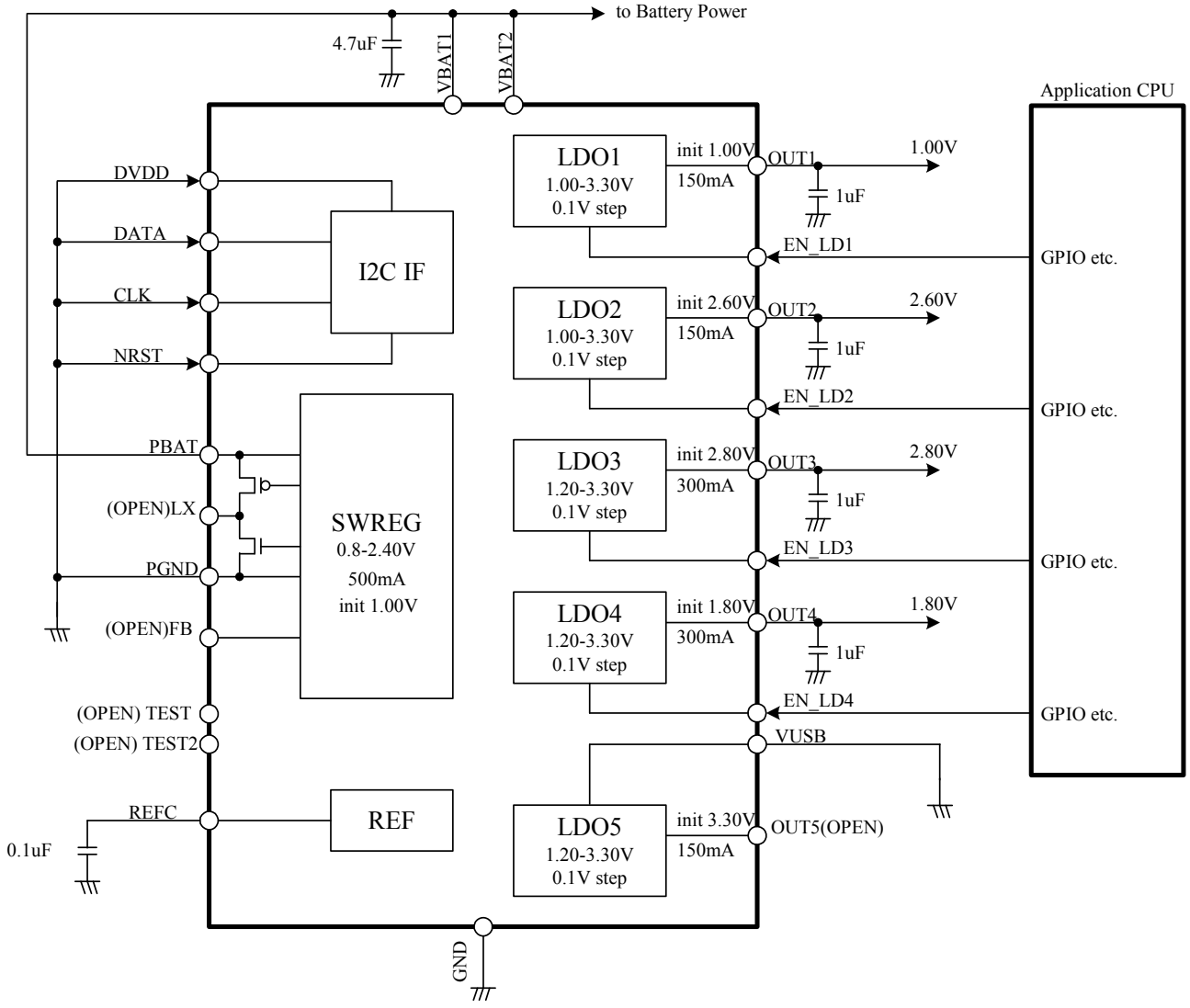


Figure 17 Application example for I2C-free mode

2-1(b) Boot sequence example 3
<Condition Sample>
Output Voltage : SWREG=OFF
: LDO1=1.00V
: LDO2=OFF
: LDO3=2.80V
: LDO4=1.80V
: LDO5=OFF
On Sequence : LDO1 -> LDO3 -> LDO4
Off Sequence : LDO4 -> LDO3 -> LDO1
SWREG, LDO1~5=1kohm discharge select
SWREG, LDO1~5=All discharge enabled
EN_LD1~4 enable pins enabled

<On Sequence Sample>
VBAT, VUSB, PBAT=Power Supply ON
DVDD=Power Supply ON (Can be kept OFF)
NRST=L -> H force (Can be kept L)

□EN_LD1='H' : LDO1=ON
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD3='H' : LDO3=ON
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD4='H' : LDO4=ON
~~~~~~
<Off Sequence Sample>
□EN_LD4='L' : LDO4=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD3='L' : LDO3=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD1='L' : LDO1=OFF
~~~~~~

Power ON/OFF sample 3（I2C free operation)

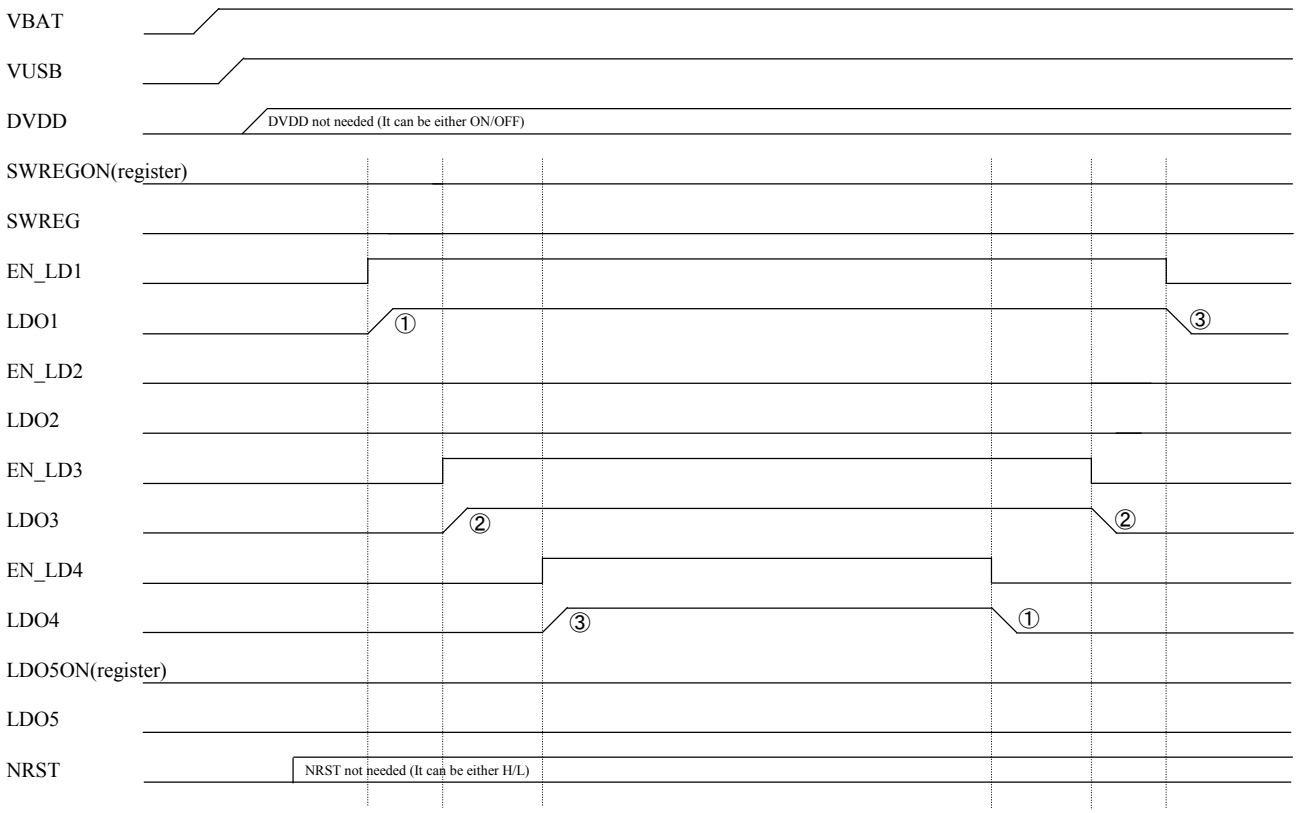


Figure 18　I2C free control ON/OFF waveform example 1

When not using the I2C interface, the DVDD power supply and the NRST pin can either be forced ‘L’ or ‘H’, since it will not be used. Keeping the pins open must be avoided because it could due to malfunction which could be caused by the surrounding severe noise.

As it is capable of booting up all LDO1~4 all at the same time, it is likely in most situations that a huge rush current will flow through each power supply. Care should be taken such as to maintain certain appropriate timing intervals between each LDO or SWREG during the boot-up sequence to avoid any unwanted drops in VBAT power supplies which may cause total system failure.

2-2(a) I2C-free mode 2 (Fixed ON mode)

LDO1~4 can only be used by the initial voltages.

All LDO1~4 will turn ON as soon as VBAT power supply is connected to the Battery Power.

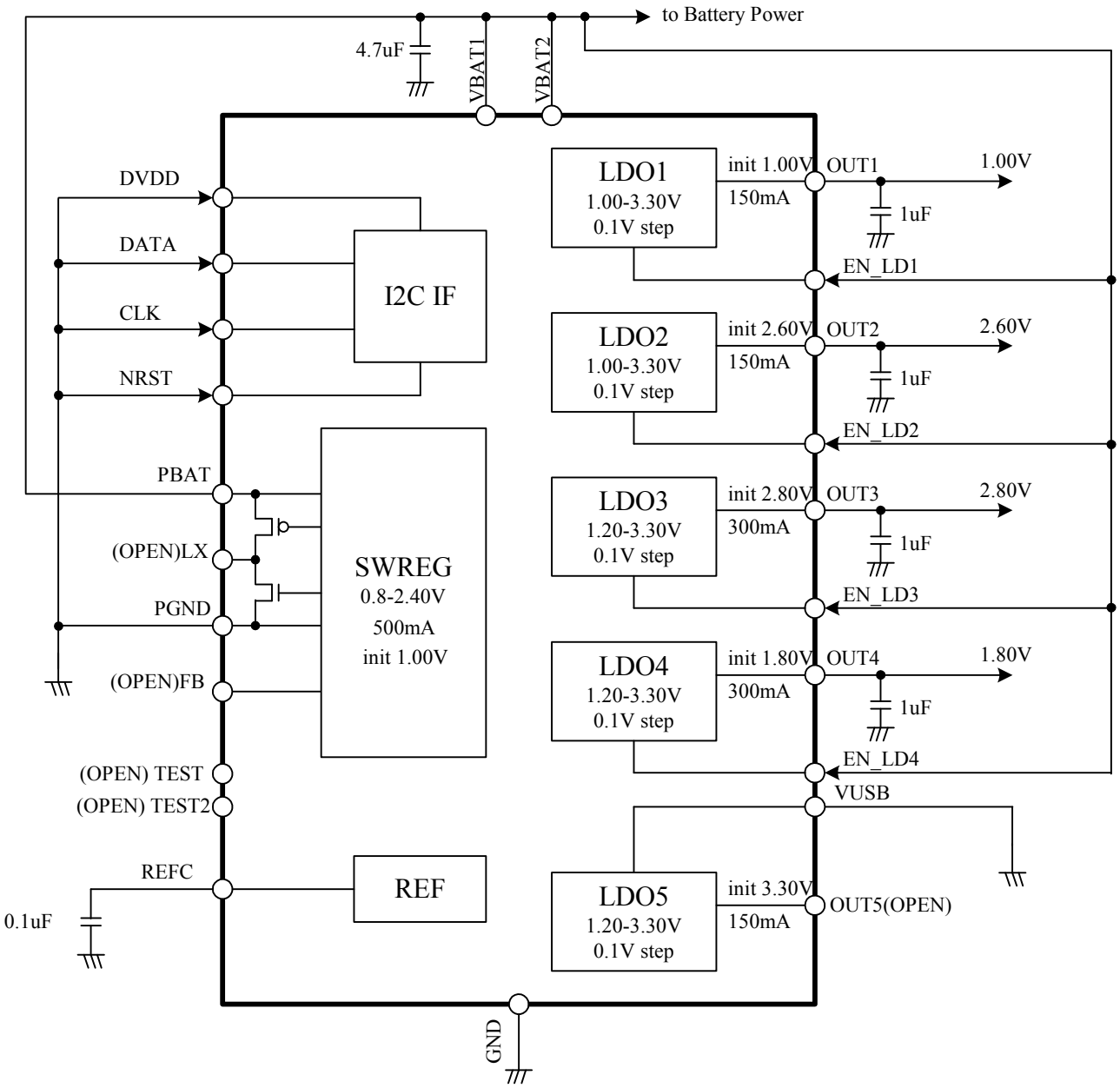


Figure 19 Application example for I2C-free mode 2

Power ON/OFF sample 4（I2C free operation 2)

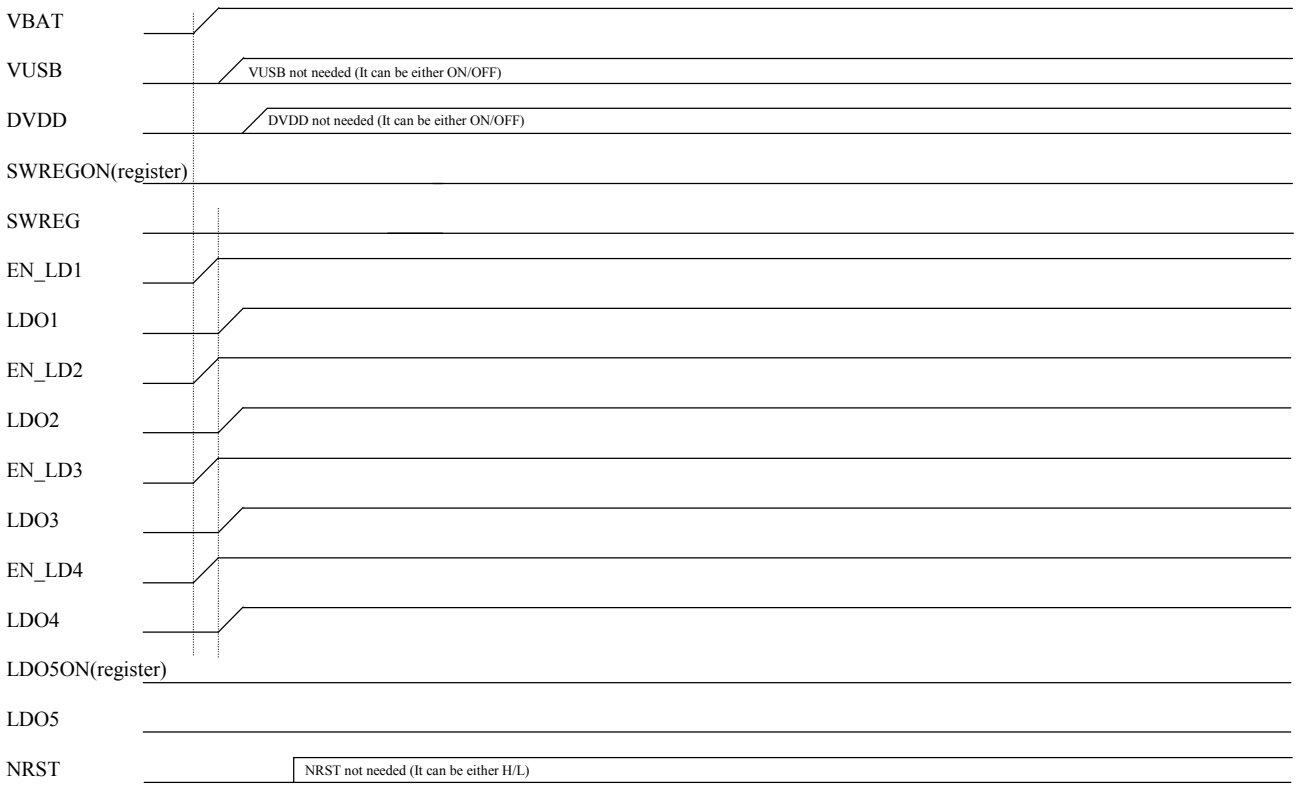


Figure 20　I2C free control ON/OFF waveform example 2

When not using the I2C interface, the DVDD power supply and the NRST pin can either be forced ‘L’ or ‘H’, since it will not be used. Keeping the pins open must be avoided because it could due to malfunction which could be caused by the surrounding severe noise.

When booting up LDO1~4 all at the same time, it is likely in most situations that a huge rush current will flow through each power supply. Care should be taken in monitoring any drops in VBAT power supply which may cause total system failure.

3-(a) Enable Pin control & I2C hybrid control

LDO1~4 can be freely turned ON/OFF by the corresponding enable pins EN_LD1~4.

LDO1~4 can be controlled by the I2C register if desired.

LDO1~4 enable selection can be individually controlled by the enable pin or I2C register.

LDO5, SWREG can be turned ON/OFF by the I2C interface.

Any boot sequence can be performed by the external Application CPU etc, or also by the I2C register if selected.

The output voltages can be changed freely on all LDO1~5, and also SWREG.

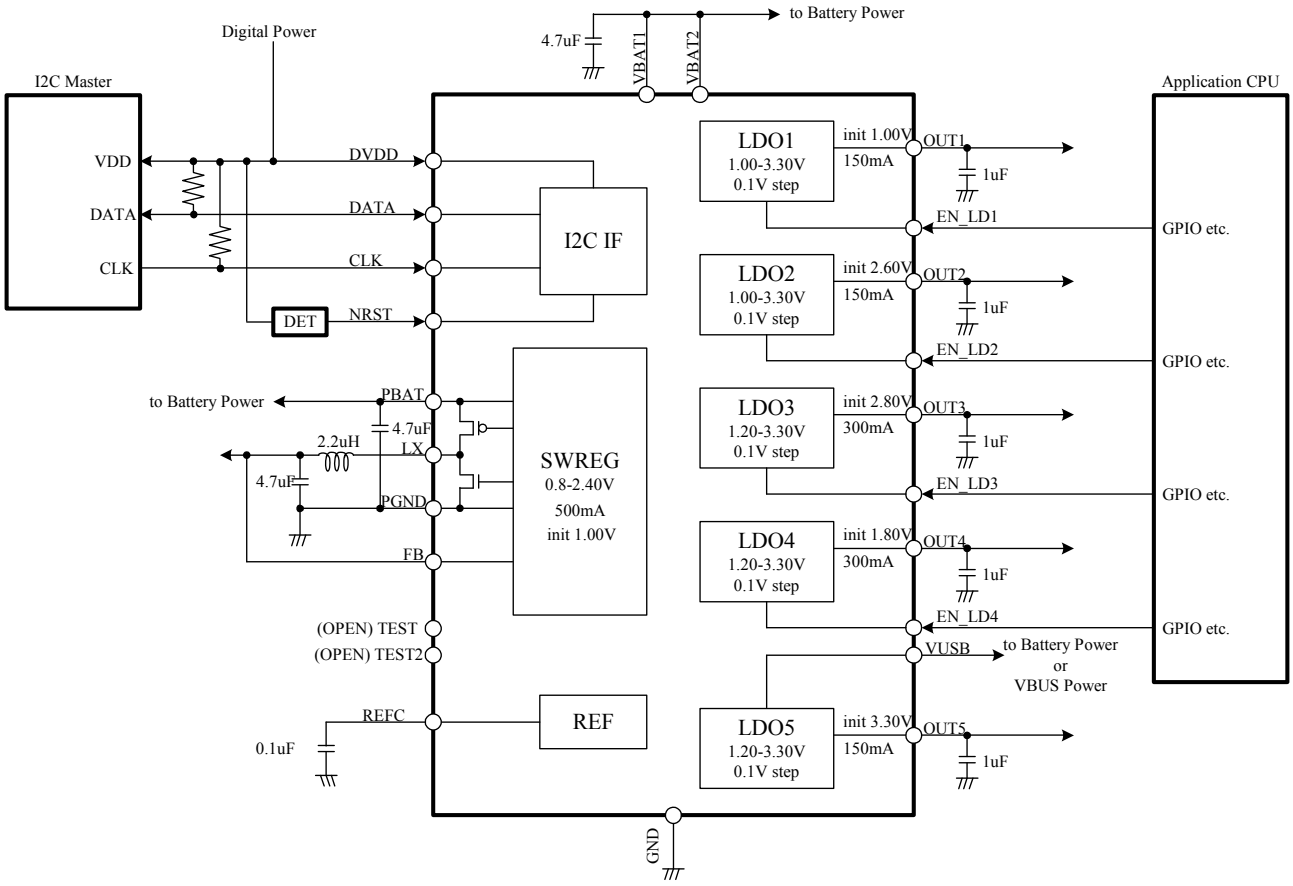


Figure 21 Application example for I2C+Enable pin mode

3-(b) Boot sequence example
<Condition Sample>
Output Voltage : SWREG=1.20V, LDO1=1.00V, LDO2=2.80V, LDO3=2.60V, LDO4=1.80V, LDO5=2.80V
On Sequence : SWREG -> LDO1, 3 -> LDO4 -> LDO2 -> LDO5
Off Sequence : LDO5 -> LDO2 -> LDO4 -> LDO1, 3 -> SWREG
SWREG, LDO1~5=1kohm discharge select
SWREG, LDO1~5=All discharge enabled

<On Sequence Sample>
VBAT, VUSB, PBAT=Power Supply ON
EN_LD1~4=L force
DVDD=Power Supply ON
NRST=L -> H force
I2C: Address=01h, Data=08h : SWREG=1.20V setting
I2C: Address=02h, Data=C0h : LDO1=1.00V, LDO2=2.80V setting
I2C: Address=03h, Data=6Ah : LDO3=2.60V, LDO4=1.80V setting
I2C: Address=04h, Data=0Ch : LDO5=2.80V setting
I2C: Address=05h, Data=00h : SWREG, LDO1~5=1kohm discharge setting
I2C: Address=06h, Data=3Fh : SWREG, LDO1~5=All discharge enabled
I2C: Address=07h, Data=00h : LDO1~4=ON/OFF control performed by EN_LD1~4 pins
I2C: Address=00h, Data=40h : BGR=ON(This command is highly recommended to maintain boot stability)
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=01h : SWREG=ON
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD1, 3=H force : LDO1, 3=ON
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD4=H force : LDO4=ON
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD2=H force : LDO2=ON
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=21h : LDO5=ON
~~~~~~
<Off Sequence Sample>
□I2C: Address=00h, Data=01h : LDO5=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD2=L force : LDO2=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD4=L force : LDO4=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□EN_LD1, 3=L force : LDO1, 3=OFF
Interval time inserted (for example 1ms, minimum 0ms)
□I2C: Address=00h, Data=00h : SWREG=OFF
~~~~~~

Power ON/OFF sample 5（I2C & Enable Pin Hybrid operation)

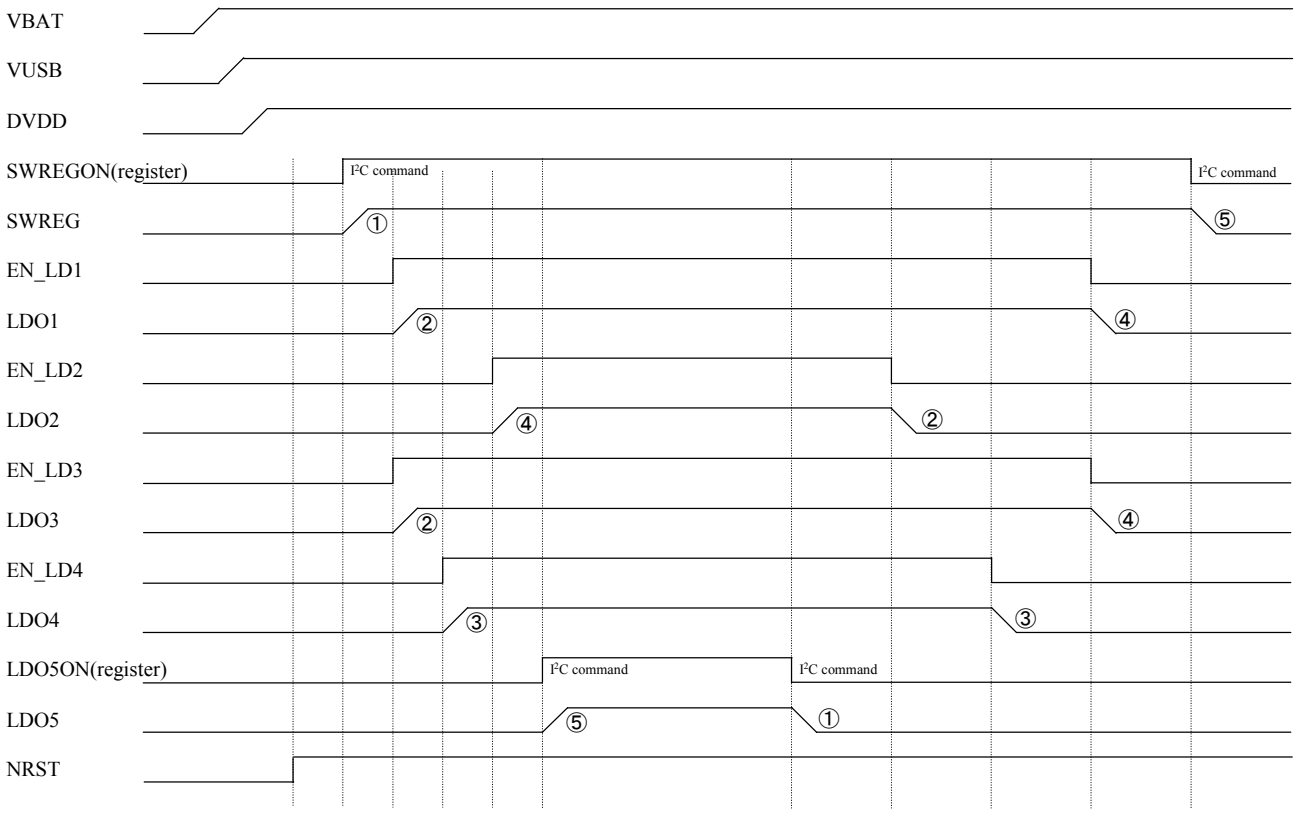


Figure 22　I2C & Enable control ON/OFF waveform example

When using EN_LD1~4 pins, it is capable of controlling the boot or off interval timing freely by the Application CPU etc.

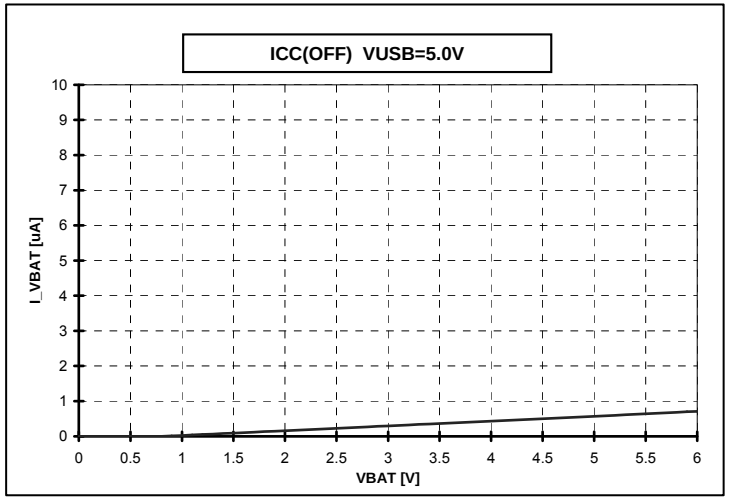
LDO5 and SWREG are only controllable by I2C, so the minimum timing interval would be approximately 23us which is dependant on the I2C CLK frequency.

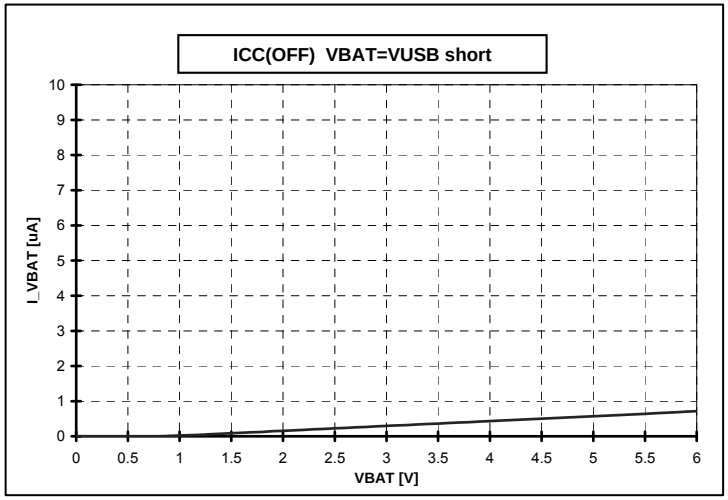
As it is capable of booting up all SWREG and LDO's all at the same time, it is likely in most situations that a huge rush current will flow through each power supply. Care should be taken such as to maintain certain appropriate timing intervals between each LDO or SWREG during the boot-up sequence to avoid any unwanted drops in VBAT power supplies which may cause total system failure.

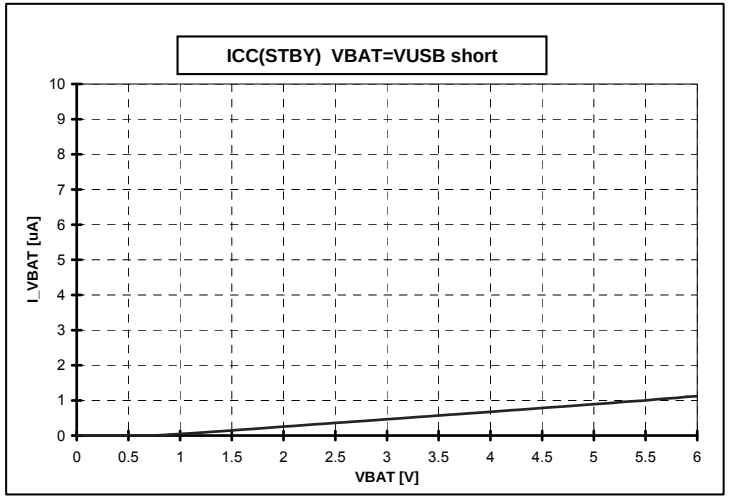
BH6172GU Evaluation Data

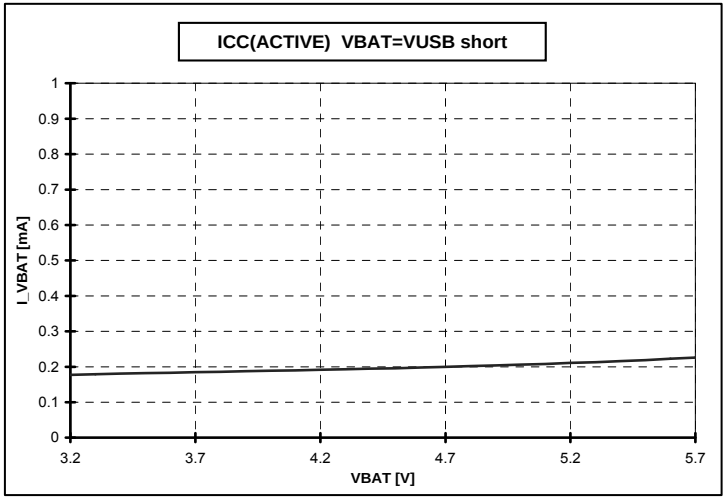
Table of contents

1. ICC

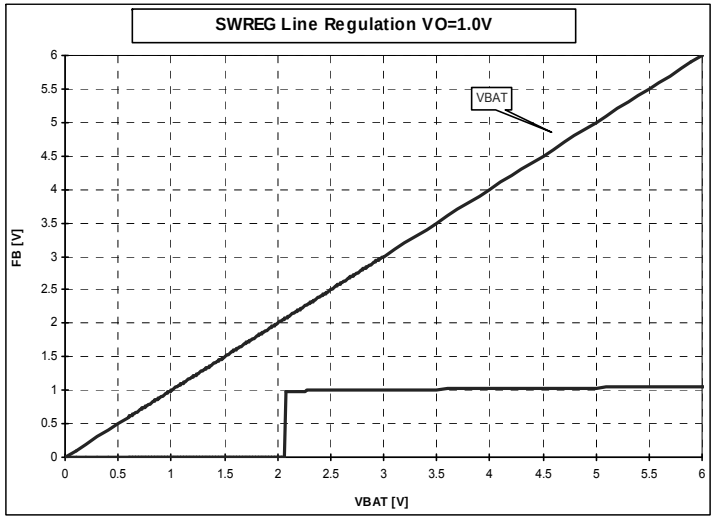

ICC(OFF) VUSB=5.0V
I_VBAT [uA]
VBAT [V]

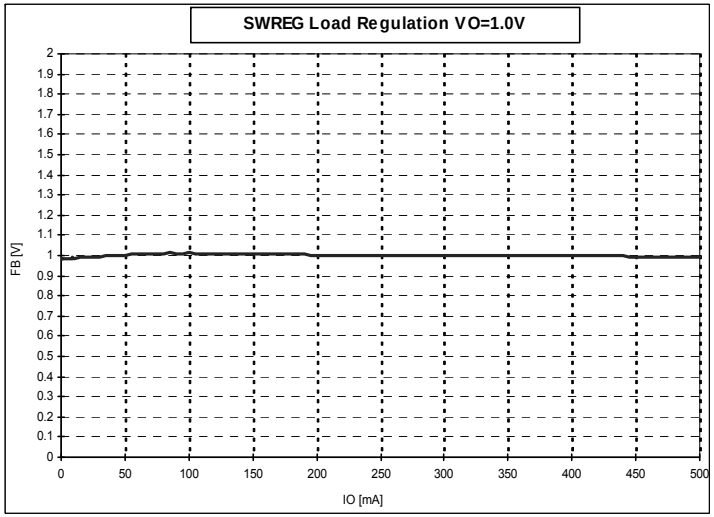

ICC(OFF) VBAT=VUSB short
I_VBAT [uA]
VBAT [V]

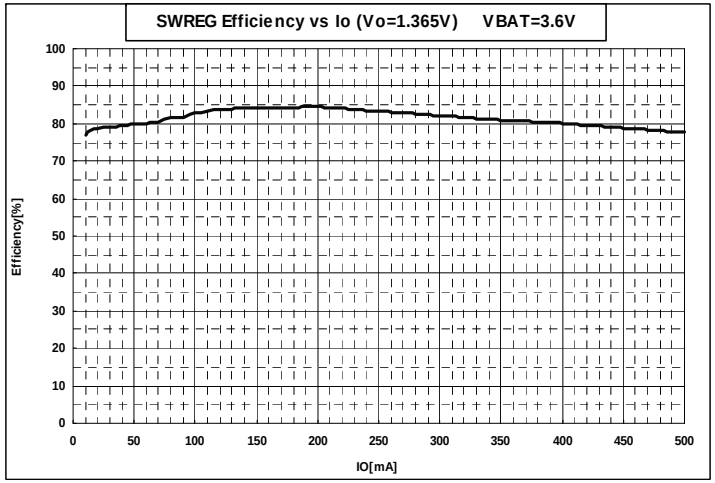

ICC(STBY) VBAT=VUSB short
I_VBAT [uA]
VBAT [V]


ICC(ACTIVE) VBAT=VUSB short
I_VBAT [mA]
VBAT [V]

2. SWREG



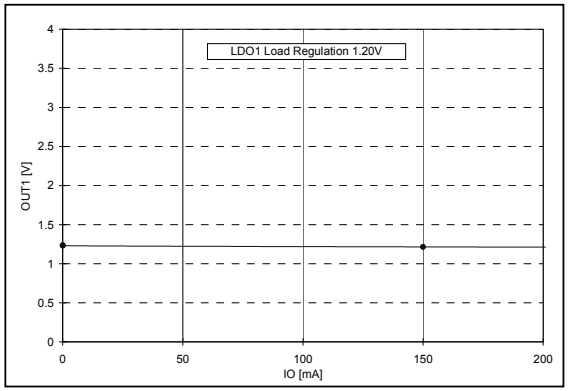


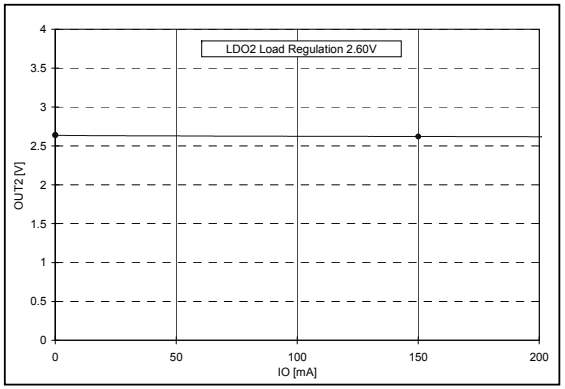


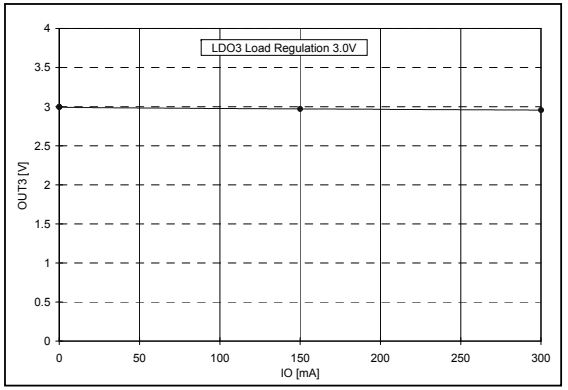
Manufacturer : FDK MIPF2016D2R2(2.2uH, 2016 size)

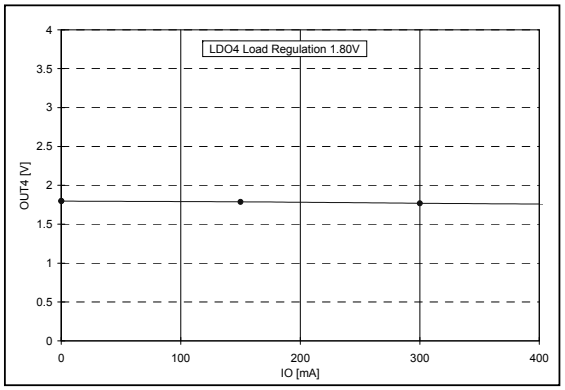
3. LDO

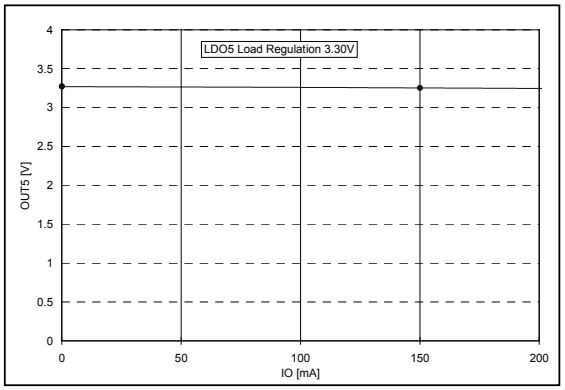
Load Regulation



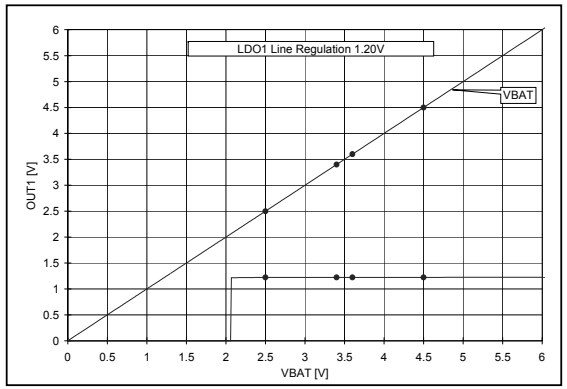


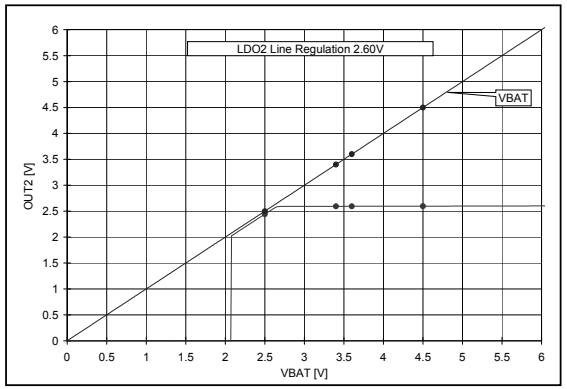


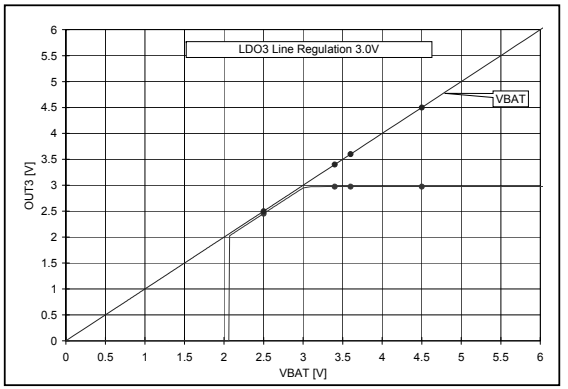


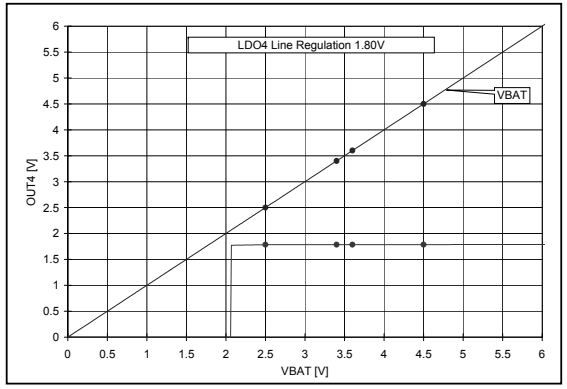


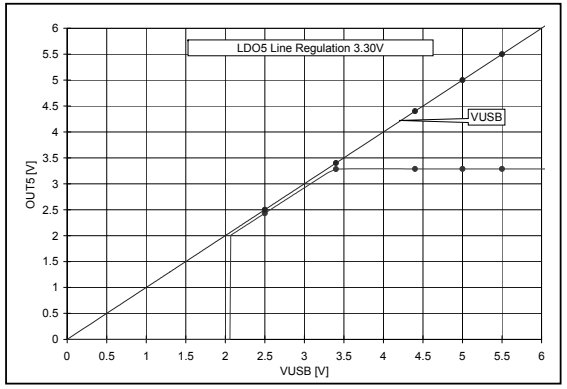
Line Regulation





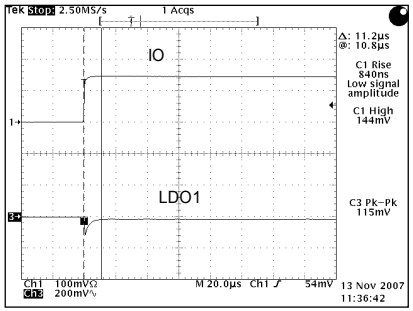


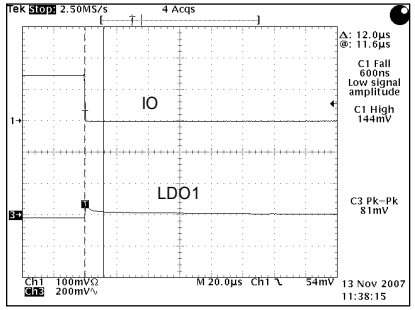




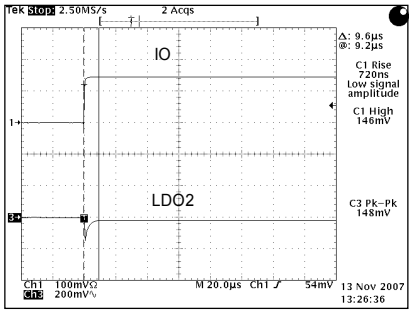
Load Change

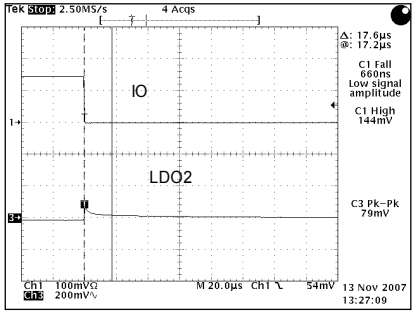
LDO1



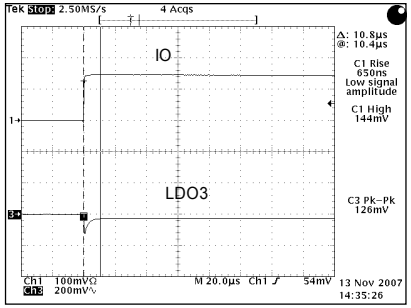


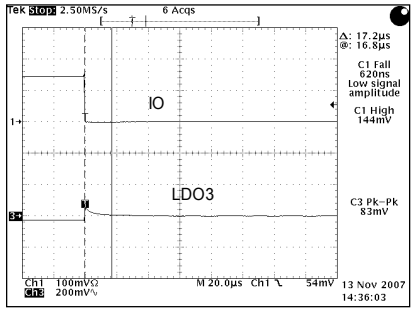
LDO2



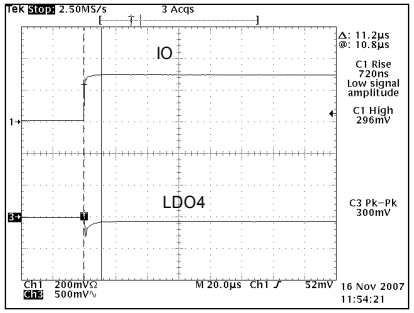


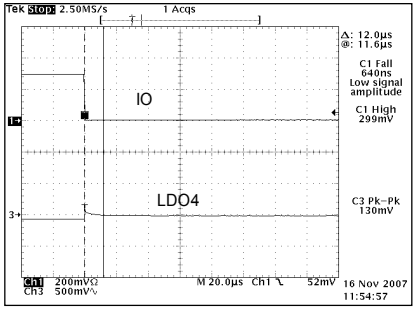
LDO3



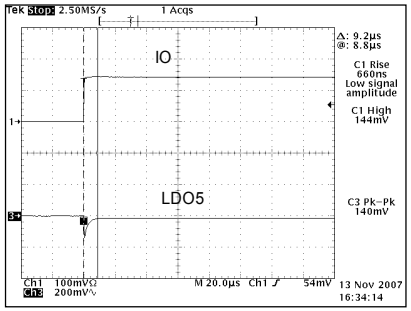


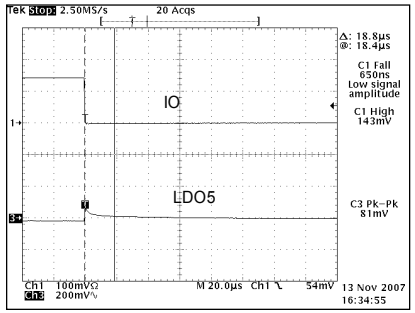
LDO4





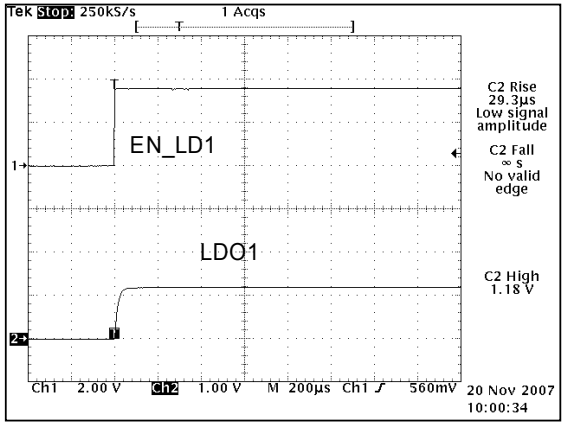
LDO5



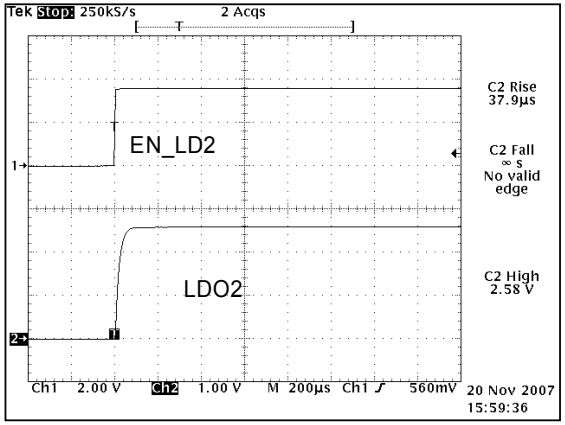


WakeUP

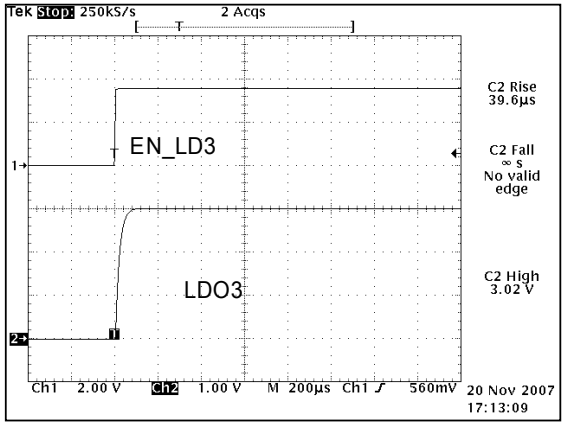
LDO1



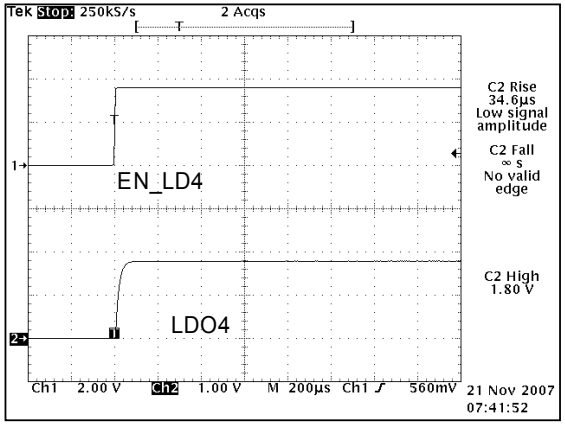
LDO2



LDO3

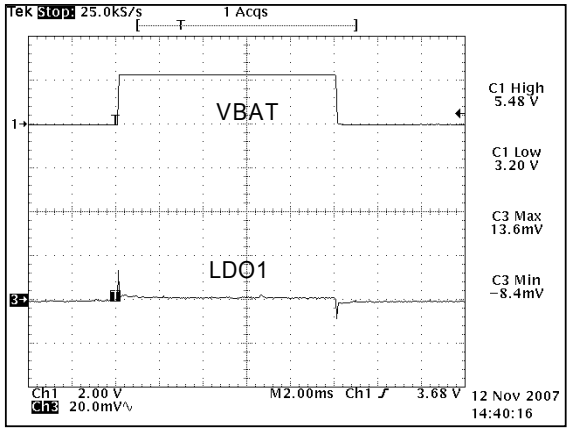


LDO4

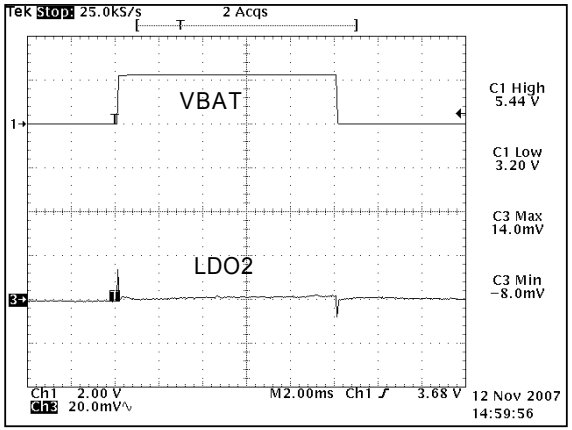


VBAT change

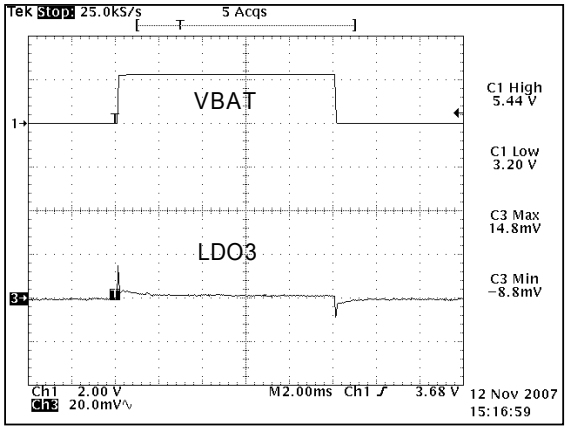
LDO1



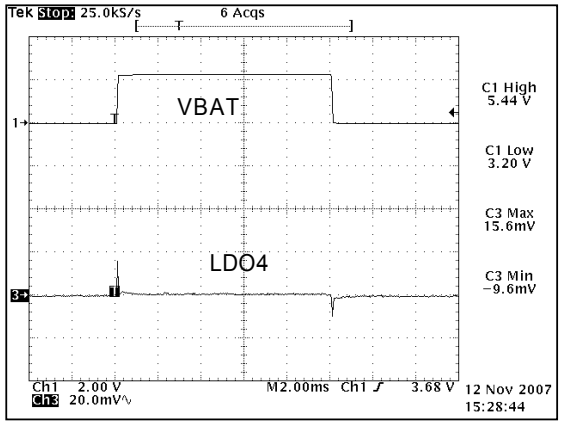
LDO2



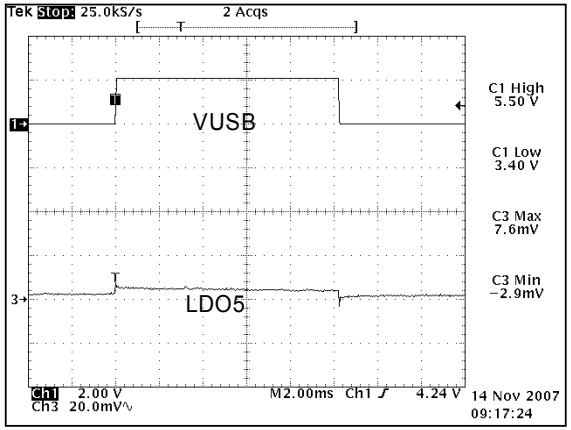
LDO3



LDO4



LDO5



BH6172GU Evaluation Board Manual

1. Requirements

This board is required the following to run properly:

< Supply list>

- Evaluation Board with the LSI mounted.
- I^2C Control Box
- 20 pin Flat cable (for connection between the Evaluation Board and I^2C Control Box)
- Control Software for transmitting I^2C command (It is packed into the CD-R.)

< Things which must be prepared >

- A PC provided with a USB port
- USB cable *
- Stabilized Power Supply

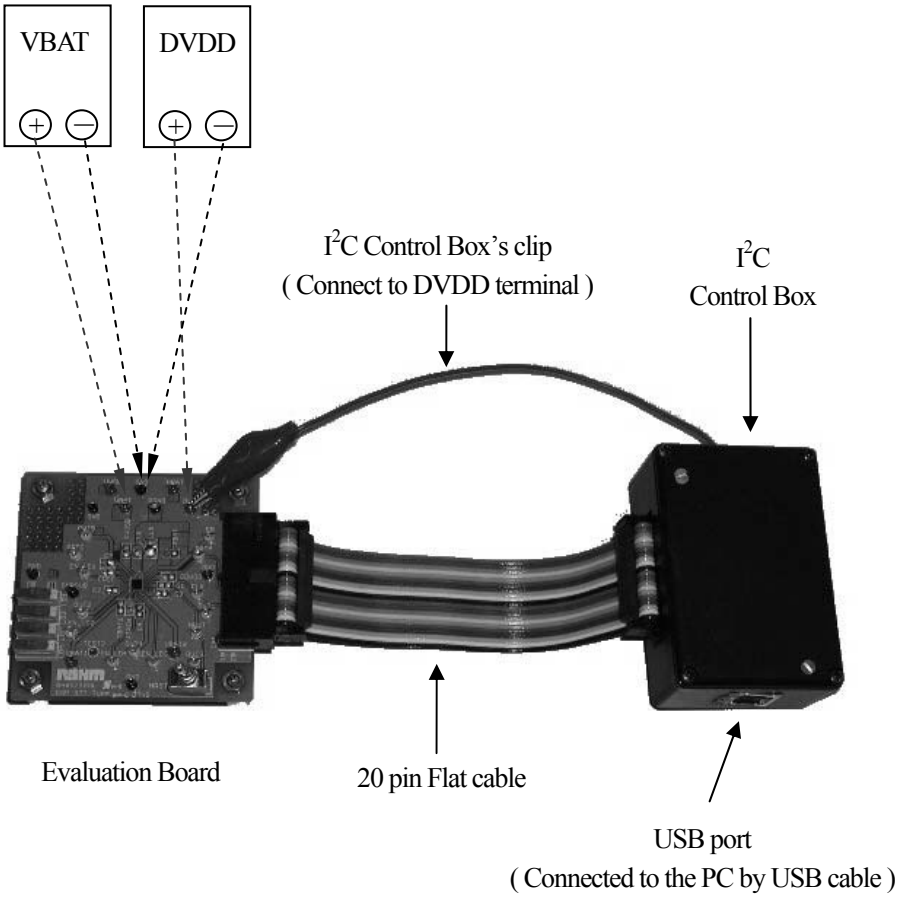
* Note: This cable is that one terminal is Standard “A” PLUG, and the other is Standard “B” PLUG.

Standard ”A” PLUG

Standard ”B” PLUG

2. Evaluation Setup image

The setup image of the evaluation is the following.



Connect a PC and the I^{2}C Control Box by using a USB cable, and connect the I^{2}C Control Box and the Evaluation Board by using the 20 pin Flat cable.

Connect the I^{2}C Control Box's clip to the DVDD terminal on the evaluation board. Because, the I^{2}C I/O level must be DVDD .

3. Setup process

1) Switch the PC ON, and install the I^2C control software.
2) Connect the evaluation board and the I^2C Control Box with the 20 pin flat cable.
3) Connect the I^2C Control Box's clip to the DVDD terminal.
4) Connect the evaluation board and the PC with a USB cable.
5) Be sure that NRST switch is L
6) Switch on the VBAT power supply. (e.g. VBAT=3.6V)
7) Switch on the DVDD power supply. (e.g. DVDD=2.6V)
8) Turn NRST switch to H (NRST = H)

4. Setup of each switch

Each switch arranged at the lower area of the Evaluation Board goes the following control.

Name	Function	Operation	
		H	L
NRST	Reset Input	Normal	Reset
LD1 *	LDO1 Power ON/OFF control	Power ON	Power OFF
LD2 *	LDO2 Power ON/OFF control	Power ON	Power OFF
LD3 *	LDO3 Power ON/OFF control	Power ON	Power OFF
LD4 *	LDO4 Power ON/OFF control	Power ON	Power OFF

*: LDO's Power ON/OFF control can be changed either by register control or external pin control by the address 07h value (EN_SEL).

5. Each functional pin

There is the following functional pin in BH6172GU.

Pin name of Board	Function
DATA	Data input/output for I^2C
CLK	CLK input for I^2C
VBAT, VBAT1, VBAT2	Main Power Supply
PBAT	Power Supply for SWREG
PGND	Ground for SWREG
FB	Voltage Feed back pin for SWREG
NRST	RESET Input Pin
OUT1	LDO1 Output
OUT2	LDO2 Output
OUT3	LDO3 Output
OUT4	LDO4 Output
OUT5	LDO5 Output
REFC	Reference Voltage Output
EN_LD1	LDO1 Enable Pin
EN_LD2	LDO2 Enable Pin
EN_LD3	LDO3 Enable Pin
EN_LD4	LDO4 Enable Pin
VUSB	Power Supply for LDO5
DVDD	Digital Power Supply
GND, GNDSUB	Analog Ground

6. About the outside parts

Don't mistake an installation direction and pressure of the element, referring to the PCB circuit diagram when you replace the outside parts.

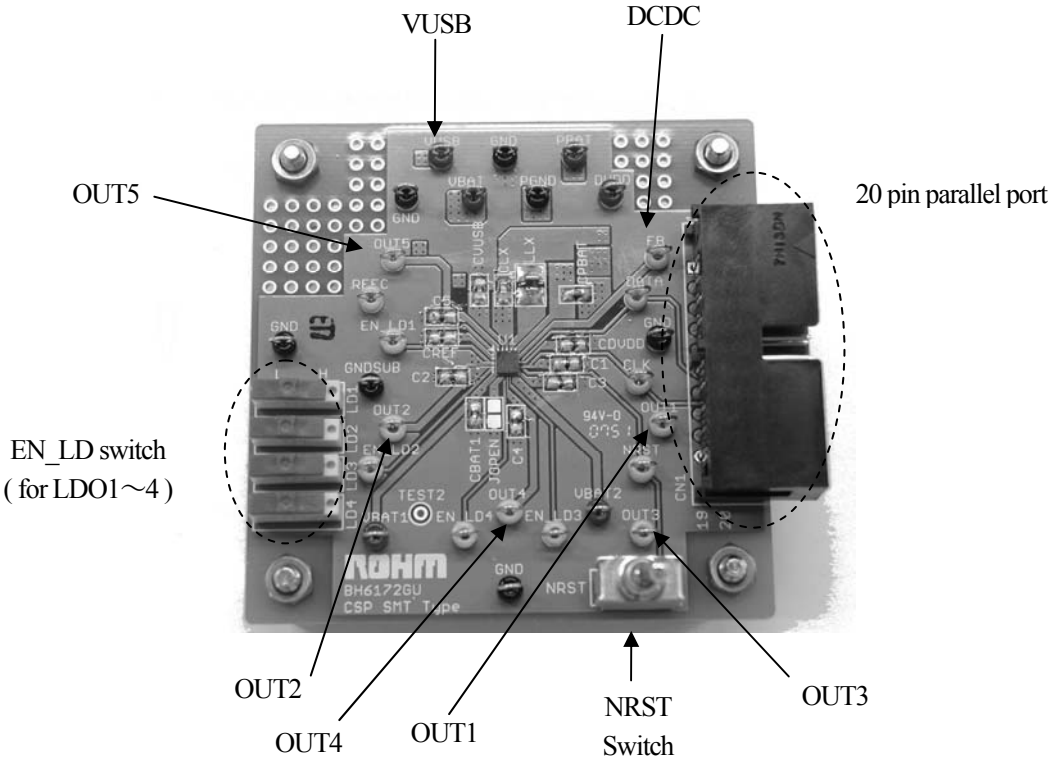
7. Note

▪ Be careful not to short-circuit the nearby pin when you monitor it.

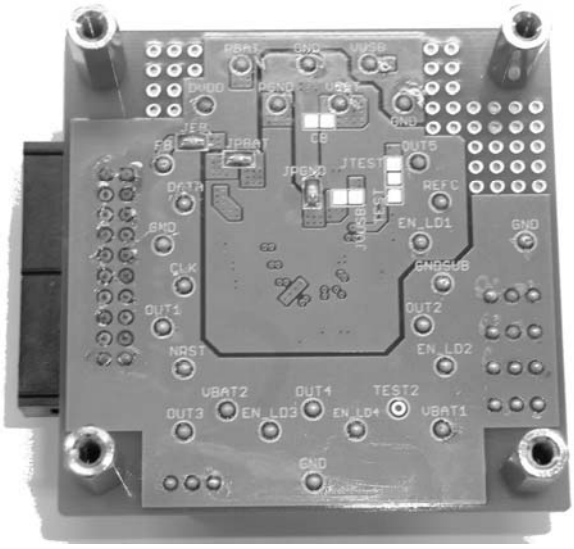
▪ Supply voltages (VBAT and DVDD) must not exceed the maximum rated value of the IC.
It can permanently destroy the IC.

8. Evaluation Board appearance

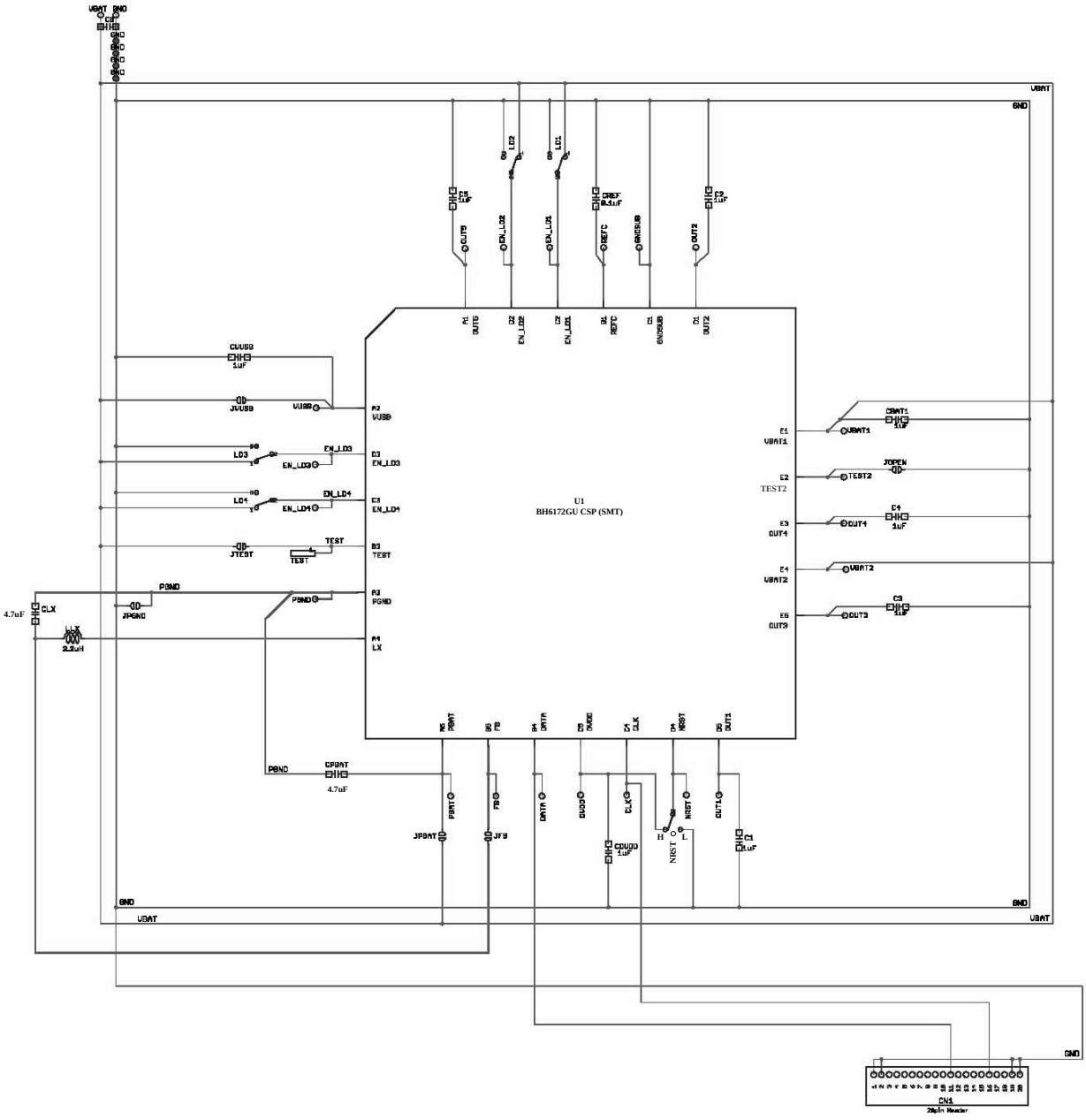
<Surface>



<Back>



9. PCB circuit diagram



I²C Control Board Manual

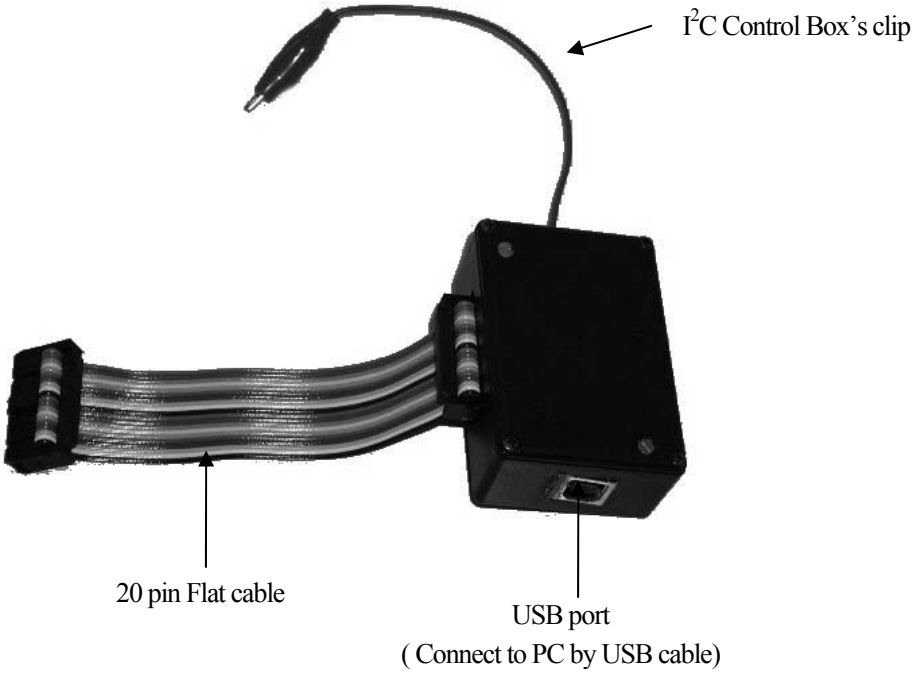
1. I²C Control Box Outline

It is the bridge box to control the LSI with the I²C format signal from the PC. An interface with the PC is done by USB. The register command transmitted by software is changed into the I²C format signals by this control box, and a command is transmitted to the LSI.

It is possible that using an exclusive software makes I²C control more easily, and the evaluation of the LSI is done more speedily. I²C interface level is supplied by connecting the I²C I/O Clip to I²C I/O level supply.

2. Appearance figure of the board

This is the appearance figure of the I²C Control Board.



3. How to use

The I²C control box and the PC are connected with a USB cable.
The I²C control box and the LSI evaluation board are connected with the 20pin flat cable.
I²C I/O Clip is connected to the I²C I/O level supply. (DVDD)
Use by provided dedicated software. (Refer to a manual for software separately.)

I²C Control Software Manual

1. Software Description

The Control Software is an integrated tool for the BH6172GU integrated circuit. With the I²C Controller board, the software sends or receives data through its I²C interface.

The major features of the control software are the following:

- User-input data validation.
- Program settings can be saved to file.
- Can automatically save write and read values to a file.
- Has a USB status indicator that tells if the correct USB device is connected to the PC.

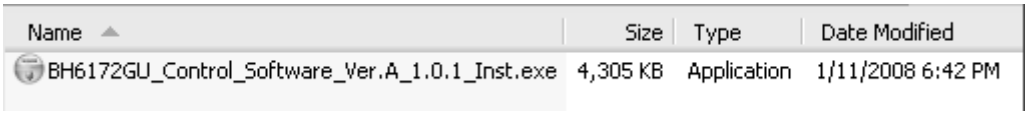
2. Requirements

This software requires the following to run properly:

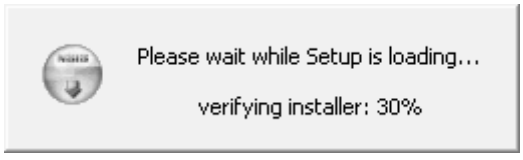
- IBM PC (At least Pentium 2 recommended)
- Windows 98/ME/2000/ XP
- Administrator privileges when installing
- I²C Controller board with Cypress CY7C68013 chip (BlackBox)
- Cypress USB driver

As a pre requisite of any .NET application, the .NET Frameworks must be installed for this software to be executed.

3. Software Installation



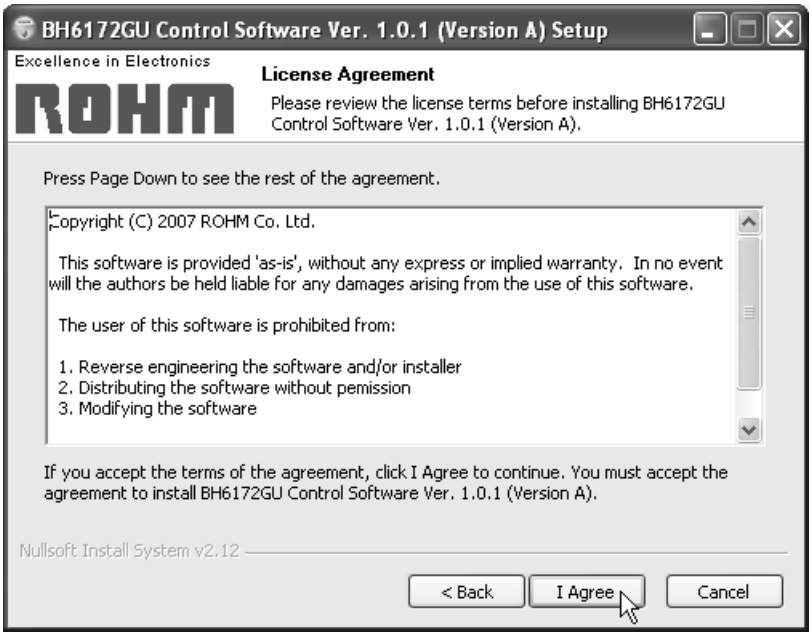
To install the application, execute the installer application BH6172GU_Control_Software_Ver.X_X_X_X.exe (where x_x_x_x=version number, e.g. BH6172GU_Control_Software_verA.1.0.0.exe for Version A 1.0.0).



The DotNET_Framework is not included on this Installer. The user needs to install the Microsoft .NET Framework separately into the computer. If the framework is already been installed in the computer, there is no need to install manually the .NET framework.

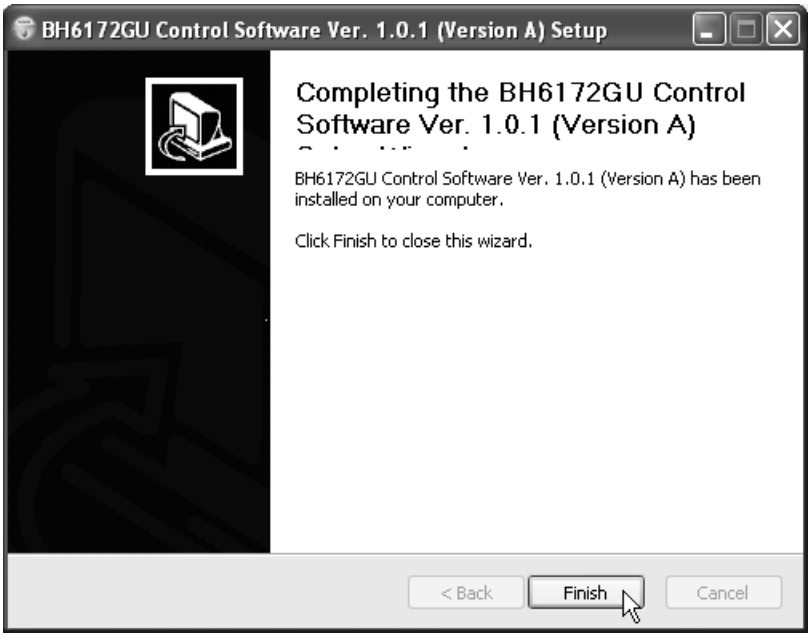
a. Follow the on-screen instruction to proceed with the installation.

b. Browse and read the License Agreement. Then click **"I agree"** if the user agrees with the agreement for the installation of this software.



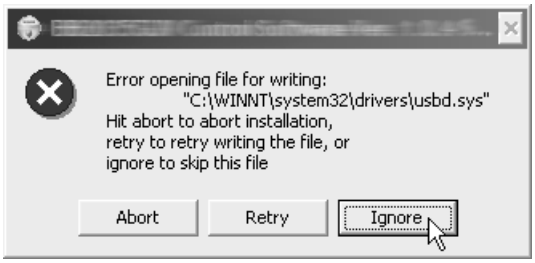
c. Click **"Browse"** to change the installation folder. Then click **"Install"** to continue the installation.

d. It is highly recommended to reboot your system upon installation of the software. Click **"Finish"** to finish the installation setup.



Then, BH6172GU Control Software Version X.1.x.x is installed in your system. The installer places a program shortcut on Desktop and on Start Programs BH6172GU Software menu. Locate the shortcut and run the program.

Sometimes an error message like this is displayed, Clicking the Ignore button will continue the installation.



This kind of error will appear when one or more files cannot be overwritten because it already exists and it is being accessed by the system.

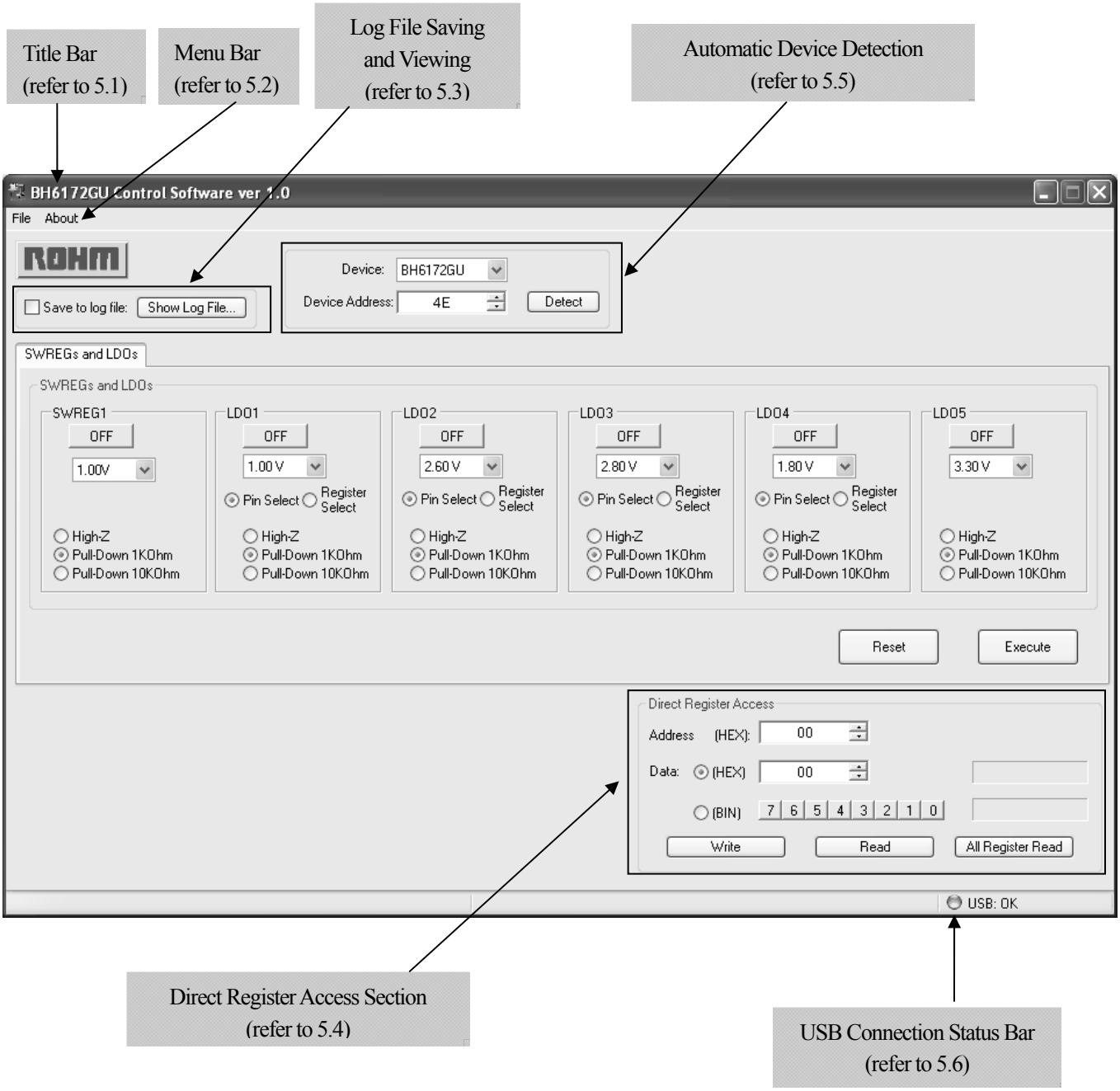
When installation is completed click the Finish button.

4. Setup of I^2C Control Board

Please refer to “BH6172GU Evaluation Board Manual”.

5. How to use

The main interface has the following parts:



Title Bar

The Title Bar displays the name/title of the application and its version, BH6172GU Control Software Ver. x.x.

Menu Bar

Click any of the choices in the main menu to display the associated pull-down command list. Then, to execute a particular function on the list, click the desired displayed command name. To close the pull-down menu, click outside the command list or press the [Esc] key.

File Menu

•Open

Opens a settings file to revert the GUI settings to a previously saved state.

•Save

Saves current state of the GUI to a settings file.

•Exit

Closes the application.

About Menu

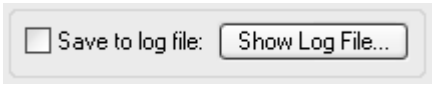
•Help

Opens a help file for the current version of software.

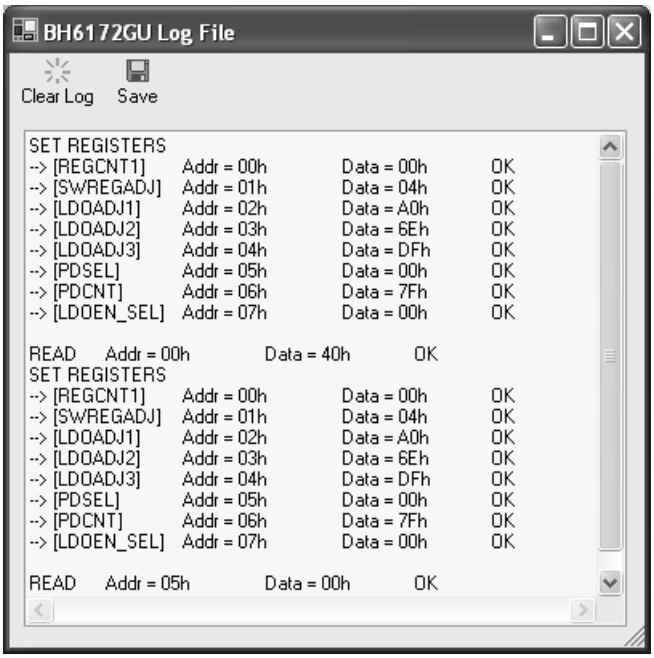
•About software

Shows information about the software (software version and author).

5.3. Show/Save Log File



When Save to log file checkbox is checked, the data which is written to, or read from the chip using any of the Execute, Reset, Set, or Read button are recorded to the “log file”.
To view the “log file” press the Show Log File button.

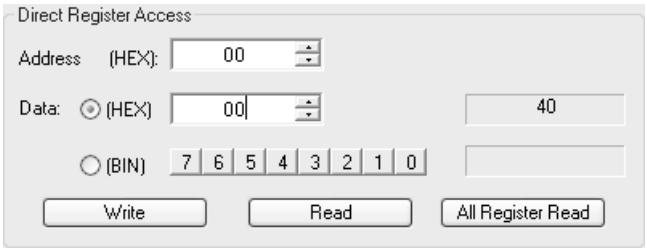


Log File Toolbar

- •Clear Log
  Clears the content of the log file
- •Save
  Saves the content of the log file

Note: The contents of the “log file” is not automatically saved to disk file, the user must use the Save button to save it.

5.4. Direct Register Access

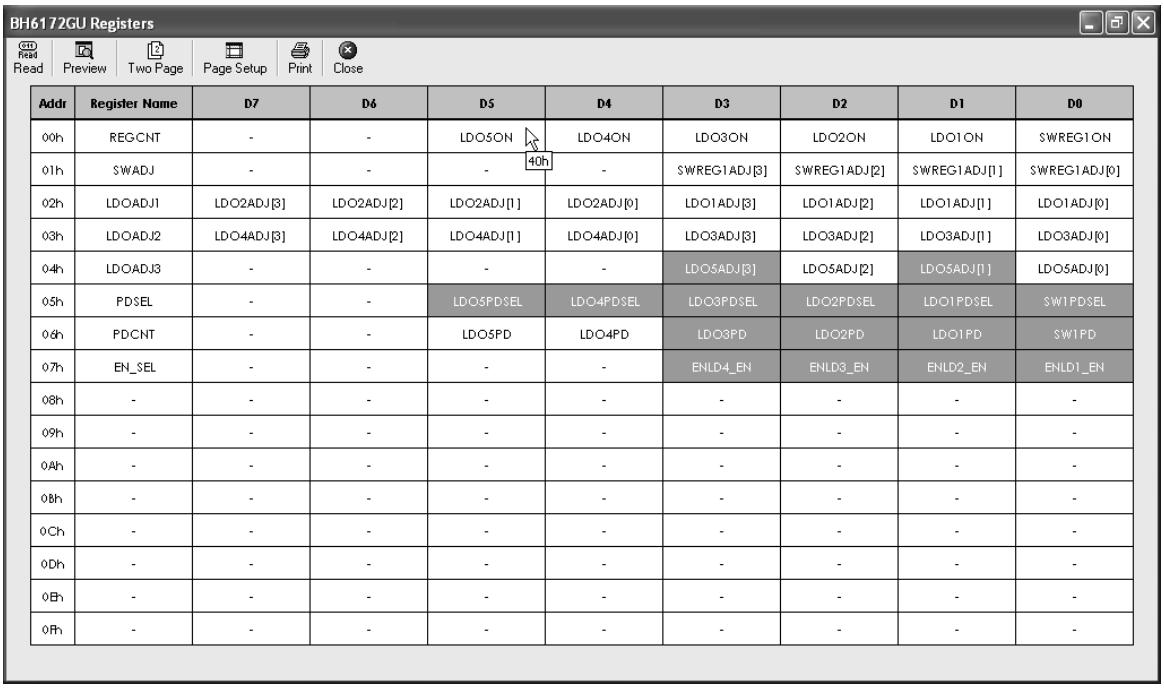


This panel enables the user to access (Write/Read) any BH6172GU register. The data format is in Hexadecimal / Binary.

1. Address spin button
   Sets the address value (in Hex).
2. Data spin button
   Sets data for the register selected (in Hex or Binary).
3. Write button
   Writes the data to the selected register address.
4. Read button
   Reads data from the selected register address and display the read data in Hex to the read display box
5. All Register Read button
   Displays read data from selected register address in Hex format.

Pressing the All Register Read button will display the BH6172GU Register table that shows the data for all registers. The register bit with a colored background indicates a value of 1 while a white background indicates a value of 0. A hard copy of the register table can be printed.

The Register table displays 00h – 0Fh registers.



Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	REGCNT	-	-	LDO5ON	LDO4ON	LDO3ON	LDO2ON	LDO1ON	SWREG1ON
01h	SWADJ	-	-	-	-	SWREG1ADJ[3]	SWREG1ADJ[2]	SWREG1ADJ[1]	SWREG1ADJ[0]
02h	LDOADJ1	LDO2ADJ[3]	LDO2ADJ[2]	LDO2ADJ[1]	LDO2ADJ[0]	LDO1ADJ[3]	LDO1ADJ[2]	LDO1ADJ[1]	LDO1ADJ[0]
03h	LDOADJ2	LDO4ADJ[3]	LDO4ADJ[2]	LDO4ADJ[1]	LDO4ADJ[0]	LDO3ADJ[3]	LDO3ADJ[2]	LDO3ADJ[1]	LDO3ADJ[0]
04h	LDOADJ3	-	-	-	-	LDO5ADJ[3]	LDO5ADJ[2]	LDO5ADJ[1]	LDO5ADJ[0]
05h	PDSEL	-	-	LDO5PDSEL	LDO4PDSEL	LDO3PDSEL	LDO2PDSEL	LDO1PDSEL	SW1PDSEL
06h	PDCNT	-	-	LDO5PD	LDO4PD	LDO3PD	LDO2PD	LDO1PD	SW1PD
07h	EN_SEL	-	-	-	-	ENLD4_EN	ENLD3_EN	ENLD2_EN	ENLD1_EN
08h	-	-	-	-	-	-	-	-	-
09h	-	-	-	-	-	-	-	-	-
0Ah	-	-	-	-	-	-	-	-	-
0Bh	-	-	-	-	-	-	-	-	-
0Ch	-	-	-	-	-	-	-	-	-
0Dh	-	-	-	-	-	-	-	-	-
0Eh	-	-	-	-	-	-	-	-	-
0Fh	-	-	-	-	-	-	-	-	-

5.5. Automatic Device Detection

Pressing the Detect button will display the device address as 4Fh if LSI setup is correct.

5.6. USB Connection Status Bar

The USB Connection Status Bar displays USB connection status.

6. Uninstalling the Software

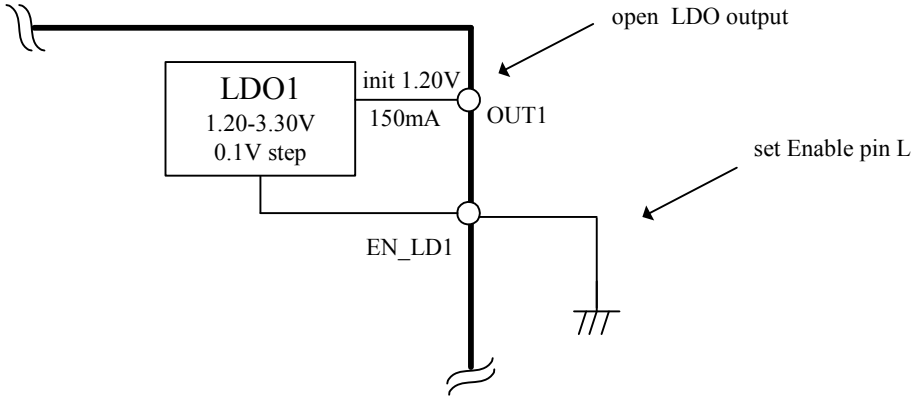
To uninstall the software, select the Uninstall from the Program shortcut in the Start menu.

USAGE NOTE

1. How to set your evaluation board If you have unused LDOs.

Remove unused LDO's capacitor refer to PCB circuit diagram.
And Set its enable switch L.
And also reminding you to not to turn on the LDO by the I^2C command.

Ex.



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ROHM CO., LTD.

21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto
615-8585, Japan
TEL: +81-75-311-2121 FAX: +81-75-315-0172
URL http: // www. rohm. com

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