ROHM SEMICONDUCTOR

Datasheet

4.75V to 18V, 2A/3A/4A 1ch Buck Converter Integrated FET

BD9325FJ BD9326EFJ BD9327EFJ

●General Description

The BD9325FJ, BD9326EFJ and BD9327EFJ are step-down regulators that integrate a low resistance high side N-channel MOSFET. It achieves 2A / 3A / 4A continuous output current over a wide input supply range. Current mode operation provides fast transient response and easy phase compensation.

●Features

- Low ESR Output Ceramic Capacitors are Available
- Low Stanby Current during Shutdown Mode
- Feedback voltage
  - 0.9V ± 1.5%(Ta=25℃),
  - 0.9V ± 3.0%(Ta=-25℃ to 85℃)
- Protection circuit:
  - Under Voltage lockout protection circuit
  - Thermal shutdown circuit
  - Over Current protection circuit

●Applications

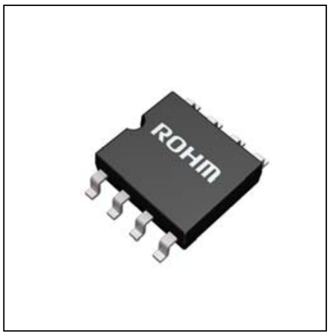
Distributed Power System
Pre-Regulator for Linear Regulator

●Key Specifications

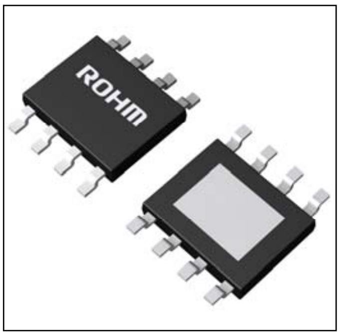
■ Input voltage range:	4.75V to 18V
■ Output currunt	
BD9327EFJ :	4.0A(Max.)
BD9326EFJ:	3.0A(Max.)
BD9325FJ:	2.0A(Max.)
■ Switching frequency:	380kHz(Typ.)
■ High Side FET ON resistance	
BD9327EFJ:	0.11Ω(Typ.)
BD9326EFJ:	0.12Ω(Typ.)
BD9325FJ:	0.16Ω(Typ.)
■ Low Side FET ON resistance:	10Ω(Typ.)
■ Standby current:	80µA (Typ.)
■ Operating temperature range:	-40℃ to +85℃

●Packages

	(Typ.) (Typ.) (Max.)
HTSOP-J8	4.90mm x 6.00mm x 1.00mm
SOP-J8	4.90mm x 6.00mm x 1.65mm

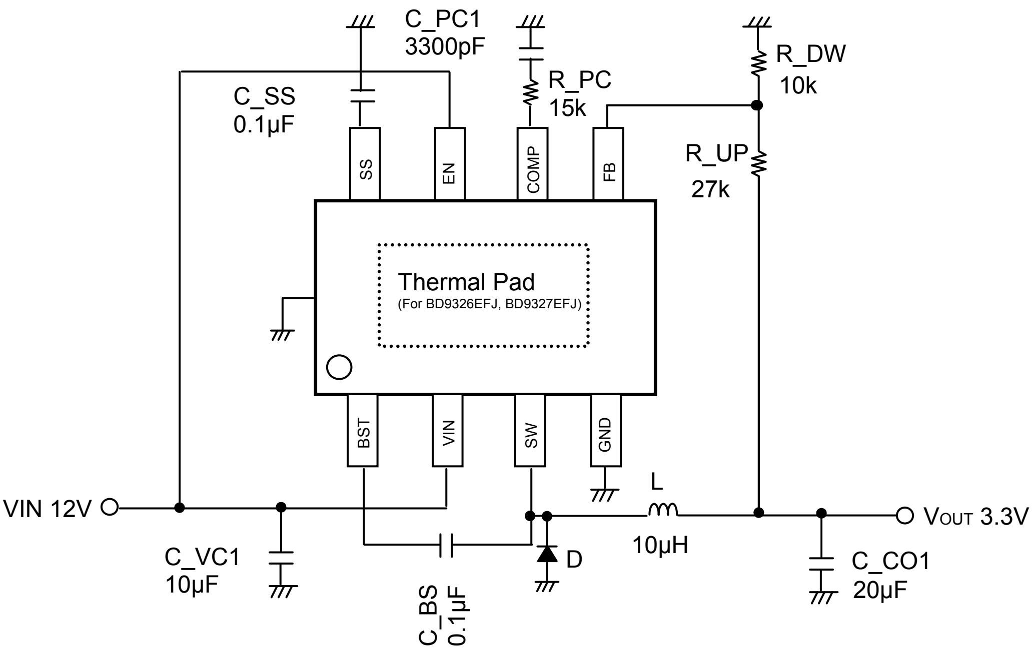


SOP-J8



HTSOP-J8

●Typical Application Circuit



○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Pin Configuration

(TOP VIEW)

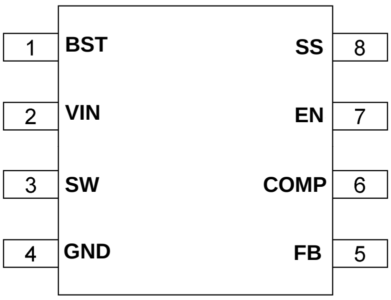


Fig.2 Pin Configuration

●Block Diagram

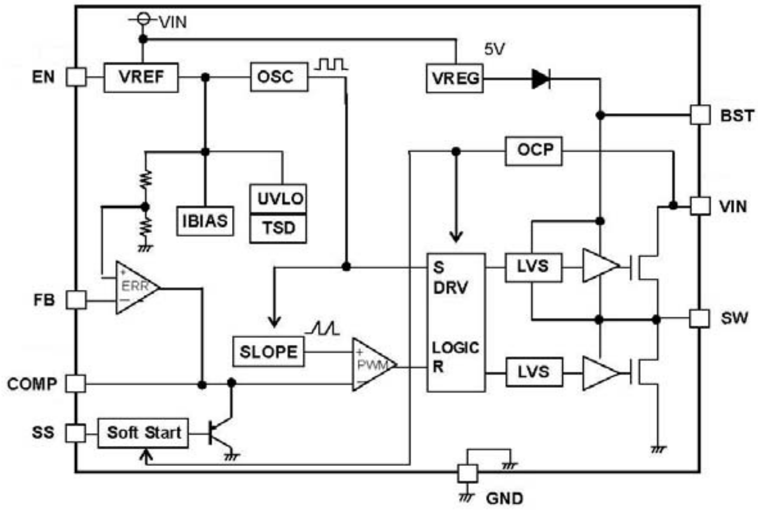


Fig.3 Block Diagram

●Pin Description

Pin No.	Pin name	Function
1	BST	High-Side Gate Drive Boost Input
2	VIN	Power Input
3	SW	Power Switching Output
4	GND	Ground
5	FB	Feed Back Input
6	COMP	Compensation Node
7	EN	Enable Input
8	SS	Soft Start Control Input

●Ordering Information

B D 9 3 2 x x x x - E 2

Part Number
BD932xxxx

Package
FJ : SOP-J8
EFJ : HTSOP-J8

Packaging and forming specification
E2: Embossed tape and reel

●Lineup

High Side FET ON resistance (Typ.)	OUTPUT CURRENT (Max.)	Package		Orderable Part Number
0.16 Ω	2.0 A	SOP-J8	Reel of 2500	BD9325FJ-E2
0.12 Ω	3.0 A	HTSOP-J8	Reel of 2500	BD9326EFJ-E2
0.11 Ω	4.0 A	HTSOP-J8	Reel of 2500	BD9327EFJ-E2

● **Absolute Maximum Ratings**(Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage [VIN]	V_{IN}	20	V
Switch Voltage [SW]	V_{SW}	20	V
Power Dissipation for HTSOP-J8	Pd1	3760 *1	mW
Power Dissipation for SOP-J8	Pd2	675 *2	mW
Operating Temperature Range	Topr	-40 to +85	℃
Storage Temperature Range	Tstg	-55 to +150	℃
Maximum junction Temperature	Tjmax	150	℃
BST Voltage	V_{BST}	V_{SW}+7	V
EN Voltage	V_{EN}	20	V
All other pins	V_{OTH}	7	V

*1 Derating in done 30.08 mW/℃ for operating above Ta≧25℃(Mount on 4-layer 70.0mm×70.0mm×1.6mm board)
*2 Derating in done 5.4 mW/℃ for operating above Ta≧25℃(Mount on 1-layer 70.0mm×70.0mm×1.6mm board)

● **Operating Ratings**(Ta= -40 to 85℃)

Parameter	Symbol	Ratings			Unit
		Min	Typ	Max	
Supply Voltage	V_{IN}	4.75	12	18	V
SW Voltage	V_{SW}	-0.5	-	18	V
Output current for BD9325FJ	I_{SW2}	-	-	2**	A
Output current for BD9326EFJ	I_{SW3}	-	-	3**	A
Output current for BD9327EFJ	I_{SW4}	-	-	4**	A

** Pd, ASO should not be exceeded

● **Electrical Characteristics**(Unless otherwise specified V_{IN}=12V Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Error amplifier block						
FB input bias current	I_{FB}	-	0.1	2	µA	
Feedback voltage1	V_{FB1}	0.886	0.900	0.914	V	Voltage follower
Feedback voltage2	V_{FB2}	0.873	0.900	0.927	V	Ta=-40℃ to 85℃
SW block – SW						
Hi-side FET On-resistance for BD9325FJ	R_{ON2}	-	0.16	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9326EFJ	R_{ON3}	-	0.12	-	Ω	I_{SW}= -0.8A ***
Hi-side FET On-resistance for BD9327EFJ	R_{ON4}	-	0.11	-	Ω	I_{SW}= -0.8A ***
Lo-side FET On-resistance	R_{ONL}	-	10	-	Ω	I_{SW}= 0.1A
Leak current N-channel	I_{LEAKN}	-	0	10	µA	V_{IN}= 18V, V_{SW} = 0V
Switch Current Limit for BD9325FJ	I_{LIMIT2}	2.5	-	-	A	***
Switch Current Limit for BD9326EFJ	I_{LIMIT3}	3.5	-	-	A	***
Switch Current Limit for BD9327EFJ	I_{LIMIT4}	4.5	-	-	A	***
Maximum duty cycle	M_{DUTY}	-	90	-	%	V_{FB}= 0V
General						
Enable Sink current	I_{EN}	86	181	275	µA	V_{EN}= 12V
Enable Threshold voltage	V_{EN}	1.1	1.18	1.4	V	
Under Voltage Lockout threshold	V_{UVLO}	4.05	4.40	4.75	V	V_{IN} rising
Under Voltage Lockout Hysteresis	V_{HYS}	-	0.1	-	V	
Soft Start Current	I_{SS}	23	41	62	uA	V_{SS}= 0 V
Soft Start Time	T_{SS}	-	1.6	-	ms	C_{SS}= 0.1 µF
Operating Frequency	F_{OSC}	300	380	460	kHz	
Circuit Current	I_{CC}	-	2.1	4.3	mA	V_{FB}= 1.5V, V_{EN}= 12V
Standby Current	I_{QUI}	-	80	170	µA	V_{EN}= 0V

*** See the lineup table .

●**Typical Performance Curves**

(Unless otherwise specified, V_{IN}= 12V Ta = 25℃)

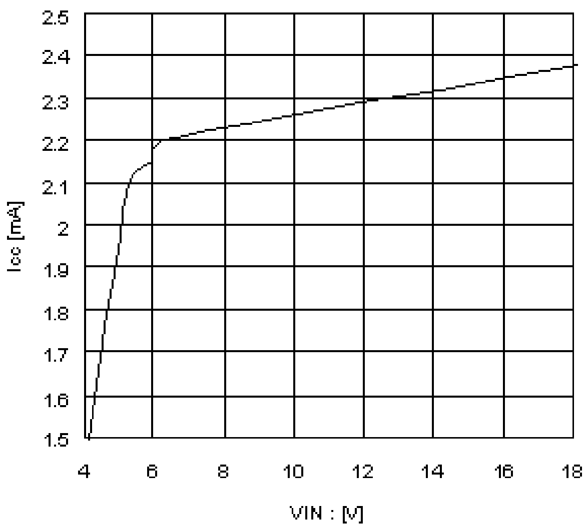


Fig.4 Circuit Current
(No switching)

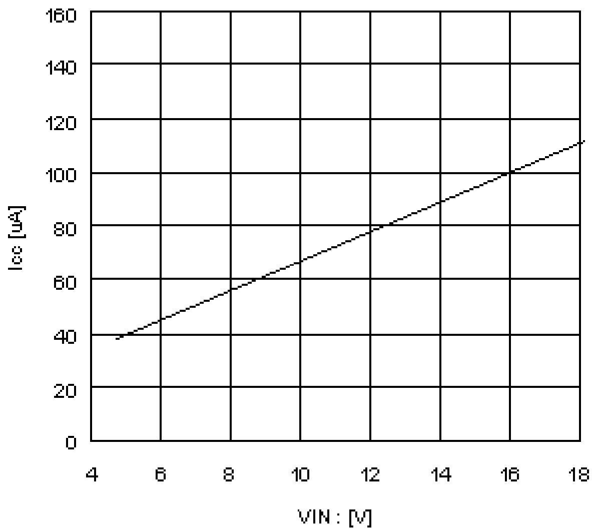


Fig.5 Quiescent Current
(IC not active)

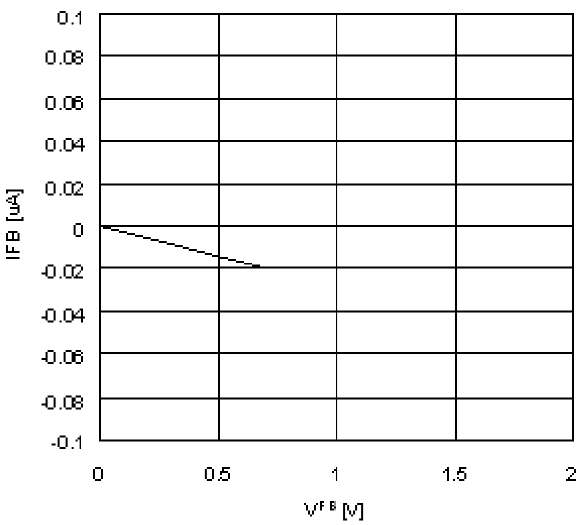


Fig.6 Input Bias Current

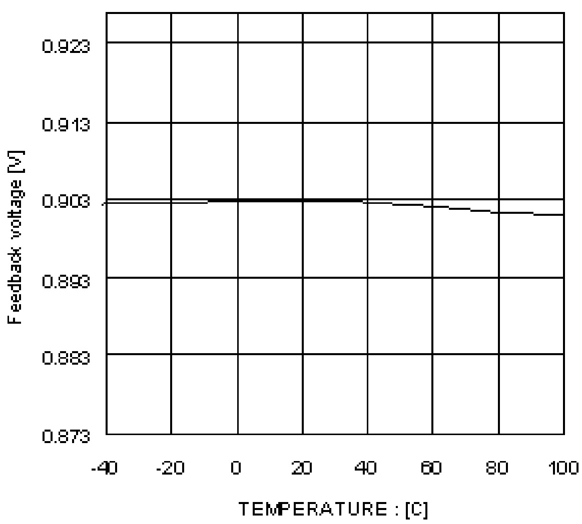


Fig.7 Feedback voltage

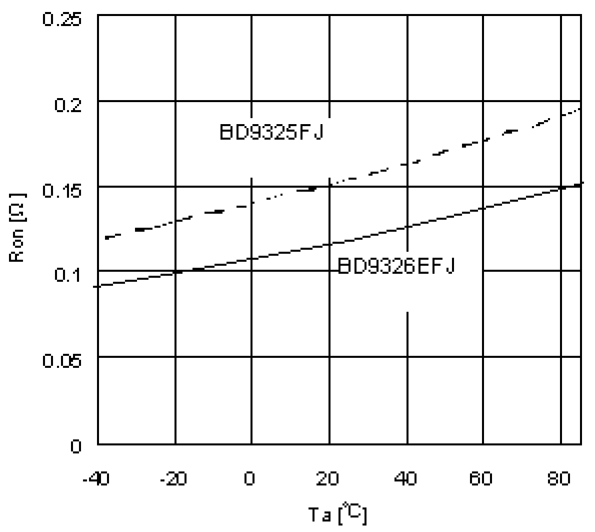


Fig.8 Hi-Side On-resistance

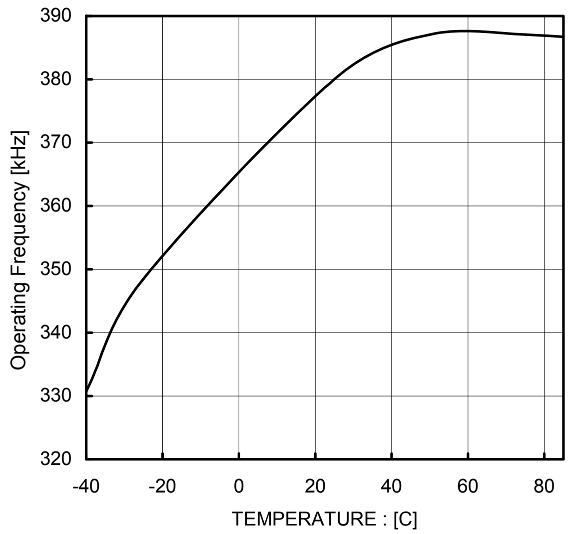


Fig.9 Operating Frequency

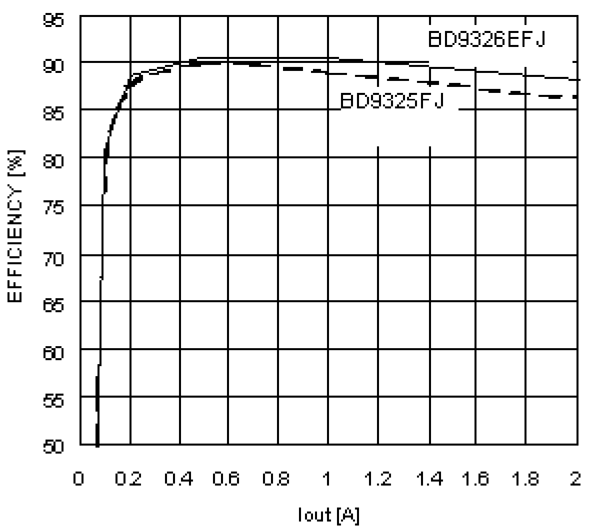


Fig.10 STEP Down Efficiency
(VIN= 12V VOUT= 3.3V L=10µH)

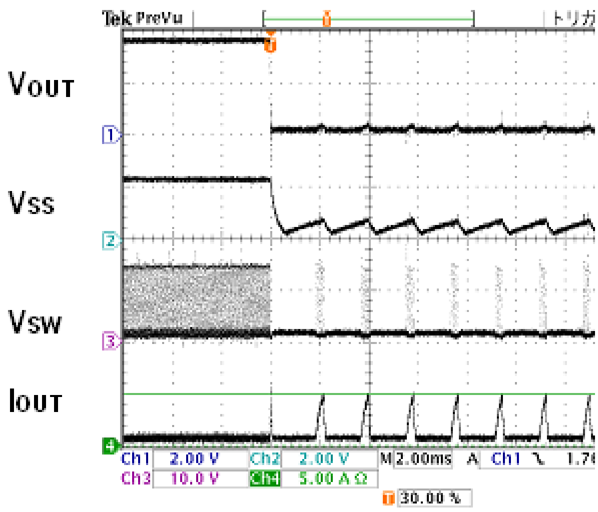


Fig.11 OverCurrent Protection
(VOUT is shorted to GND)

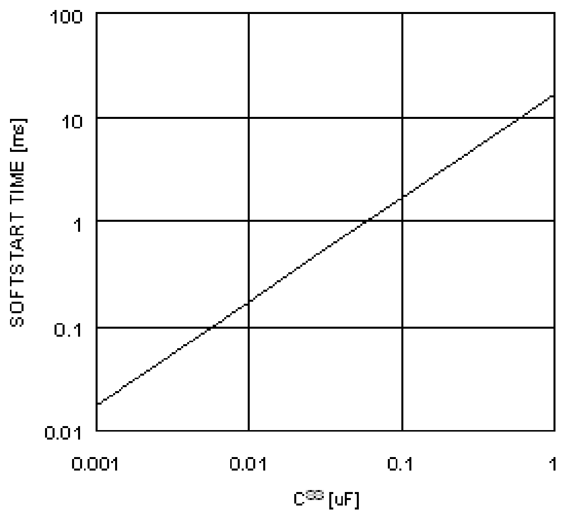


Fig.12 Soft Start Time

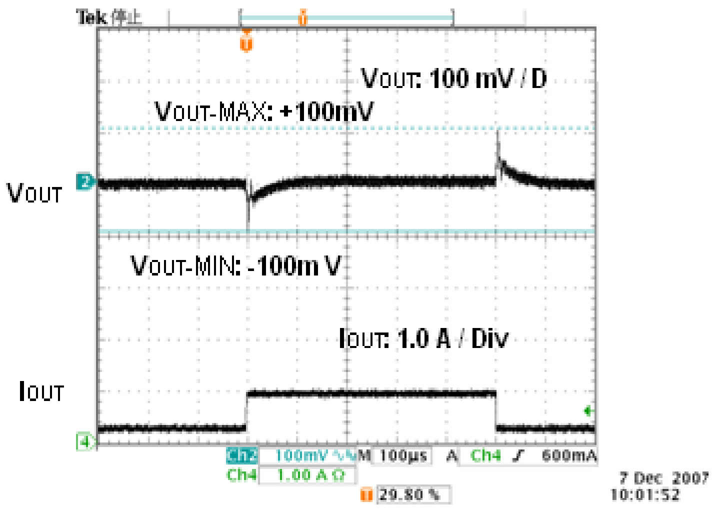


Fig.13 Transient Response
(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF Iout= 0.2-1.0A)

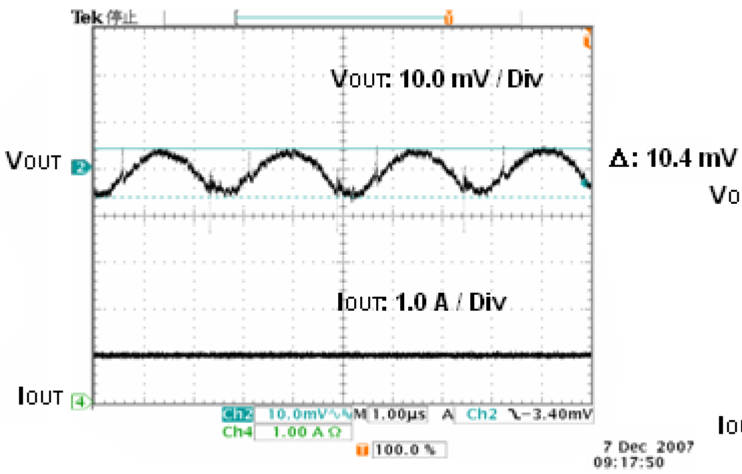


Fig.14 Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF I out= 1.0A)

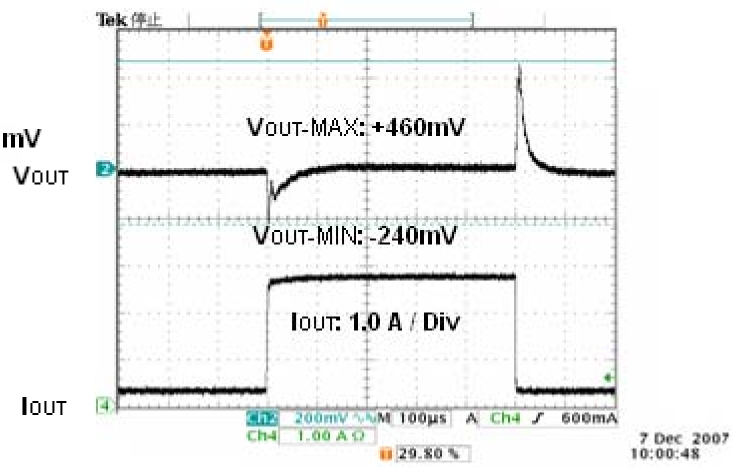


Fig.15 Transient Response
(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF Iout= 0.2-3.0A)

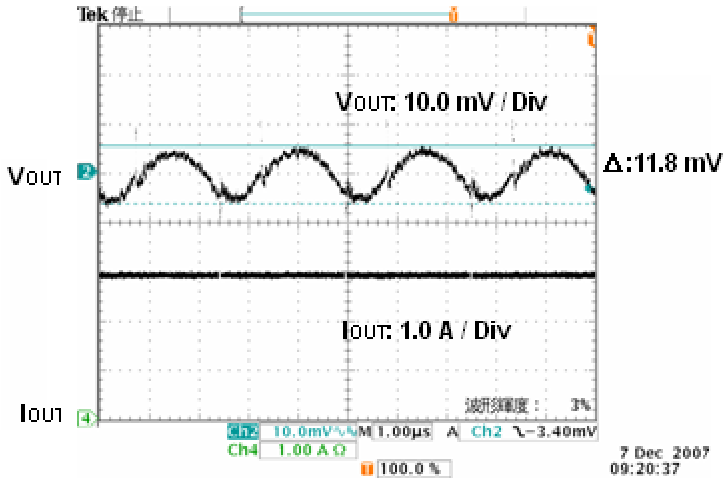


Fig.16 Output Ripple Voltage
(VIN= 12V VOUT= 3.3V L= 10µH Cout =22µF Iout= 3.0A)

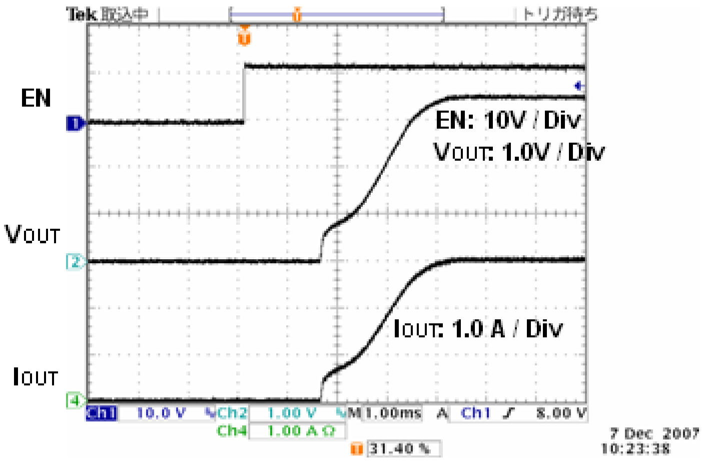


Fig.17 Start Up waveform
(VIN= 12V VOUT= 3.3V L= 22µH CSS= 0.1µF Iout= 0A)

●Application Information

Block Operation

・VREG
A block to generate constant-voltage for DC/DC boosting.

・VREF
A block that generates internal reference voltage of 2.9 V (Typ.).

・TSD/UVLO
TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175℃ (Typ.) The UVLO circuit shuts down the IC when the VIN is Low Voltage.

・Error amp block (ERR)
This is the circuit to compare the reference voltage and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

・Oscillator block (OSC)
This block generates the oscillating frequency.

・SLOPE block
This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

・PWM block
The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

・DRV block
A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

・OCP block
OCP (Over Current Protection) block. The current which flowed into FET is detected and OCP starts. After OCP, switching is turned off and SS capacitor is discharged. OCP is not latch type but auto restart.

・Soft start circuit
Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

Selecting Application Components

(1) Output LC constant (Buck Converter)

The inductance L to use for output is decided by the rated current ILR and input current maximum value IOMAX of the inductance.

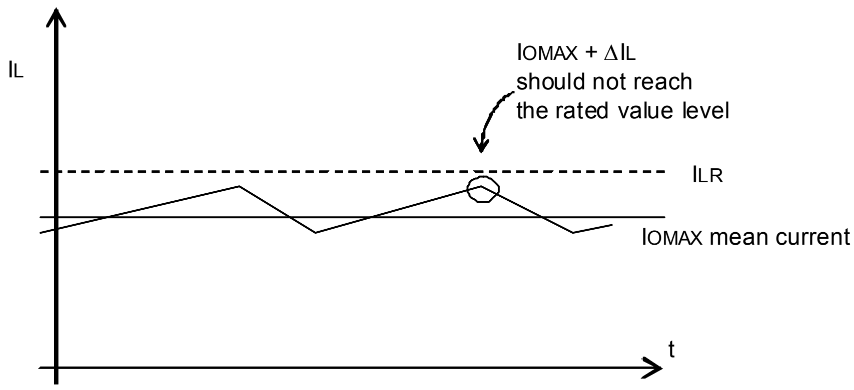


Fig.18

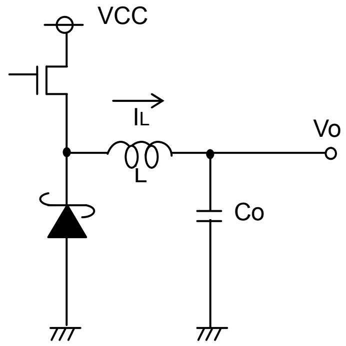


Fig.19

Adjust so that IOMAX + ΔIL does not reach the rated current value ILR. At this time, ΔIL can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (V_{CC} - V_o) \times \frac{V_o}{V_{CC}} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2Co} \times \frac{V_o}{V_{CC}} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage VDR during sudden load change, please perform the rough calculation by the following equation.

$$V_{DR} = \frac{\Delta I_L}{Co} \times 10\ \mu s \quad [V]$$

However, 10μs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2) Loop Compensation

Choosing compensation capacitor C_1 and resistor R_3

The example of DC/DC converter application bode plot is shown below. The compensation resistor R3 will set the cross over frequency FC that decides the stability and response speed of DC/DC converter. So compensation resistor R3 has to be adjusted to adequate value for good stability and response speed.

The cross over frequency F_C can be adjusted by changing the compensation resistor R3 connected to COMP terminal. The higher cross over frequency achieves good response speed, but less stability. And the lower cross over frequency shows good stability, but worse response speed.
Usually, the 1/10 of DC/DC converter operating frequency is used for cross over frequency F_C. So please decide the compensation resistor and capacitor using the following formula on setting F_C to 1/10 of operating frequency at first.
After that, please measure and adjust the cross over frequency on your set (on the actual application) to meet the enough response speed and phase-margin.

(i) Choosing phase compensation resistor R3

Please decide the compensation resistor R3 on following formula.

Compensation Resistor $R_3 = 5800 \times C_{OUT} \times F_C \times V_{OUT}$ [Ω]

Where
C_{OUT} : Output capacitor connected to DC/DC output
V_{OUT} : Output voltage
F_C : Desired cross over frequency (38kHz)

The larger R3, value of Fc increase (responce better and stability worse).
The smaller R3, value of Fc decrease (responce worse and stability better).

(ii) Choosing phase compensation capacitor C1

The stability of DC/DC converter needs to cancel the phase delay that is from output LC filter by inserting the phase advance.
The phase advance can be added by the zero on compensation resistor and capacitor.
The LC resonant frequency FLC and the zero on compensation resistor and capacitor are expressed below.

LC resonant frequency $F_{LC} = \dfrac{1}{2\pi\sqrt{LC_{OUT}}}$ [Hz]

Zero by C_1 and R_3 $F_Z = \dfrac{1}{2\pi C_1 R_3}$ [Hz]

Please choose C1 to make FZ to 1 / 3 of FLC .

Compensation Capacitor $C_1 = \dfrac{3}{2\pi F_{LC} R_3}$ [F]

(iii) The condition of the loop compensation stability
The stability of DC/DC converter is important. To secure the operating stability, please check the loop compensation has the enough phase-margin. For the condition of loop compensation stability, the phase-delay must be less than 150 degree where Gain is 0 dB. Namely over 30 degree phase-margin is needed.
Lastly after the calculation above, please measure and adjust the phase-margin to secure over 30 degree.

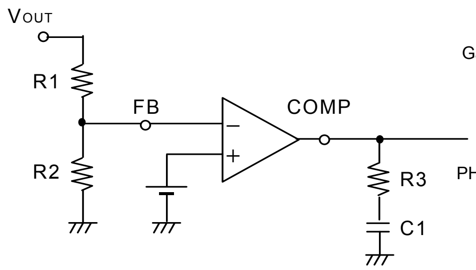


Fig.20

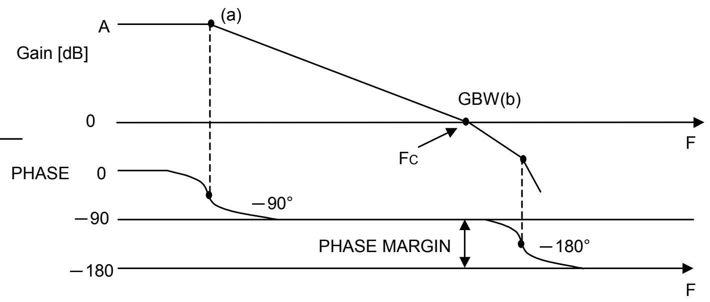
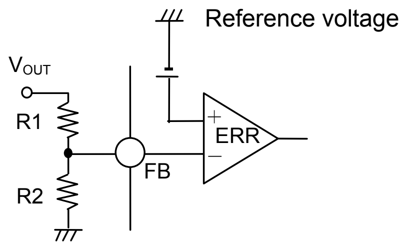


Fig.21

(3) Design of Feedback Resistance constant

Set the feedback resistance as shown below.



$V_{OUT} = \dfrac{R1 + R2}{R2} \times$ Reference Voltage [V]

Fig.22

(4)Soft Start Function

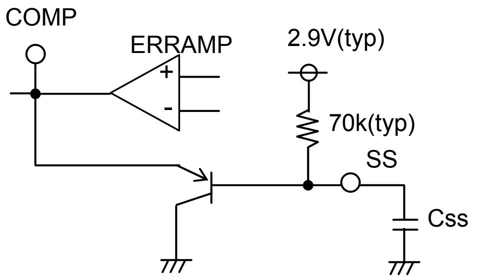


Fig.23

The buck converter has an adjustable Soft Start function to prevent high inrush current during start up.
The soft-start time is set by the external capacitor connected to SS pin.
The soft start time is given by;

Tss [ms] = 16.2・Css [μF]

Please confirm the overshoot of the output voltage and inrush current when deciding the SS capacitor value.

(5)EN Function

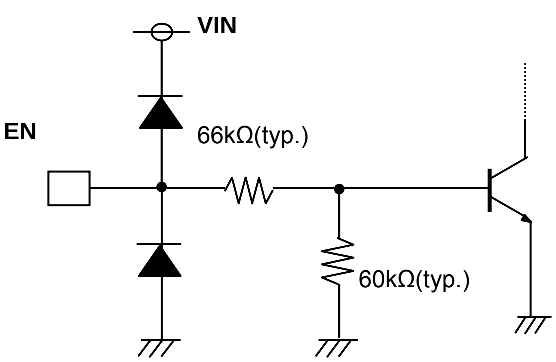


Fig.24 The equivalent internal circuit.

The EN terminal controls IC's shut down.
Leaving EN terminal open makes IC shutdown.
To start the IC, EN terminal should be connected to V_{IN} or the other power source output.
When the EN voltage exceed 1.2V (typ.), the IC start operating.

Layout Pattern Consideration

Two high pulsing current flowing loops exist in the buck regulator system.
The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND.
The second loop, when FET is OFF, starts from the shotkey diode, to the inductor, to the output capacitor, and then returns to the shotkey diode through GND.
To reduce the noise and improve the efficiency, please minimize these two loop area.
Especially input capacitor, output capacitor and shotkey diode should be connected to GND plain.
PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.

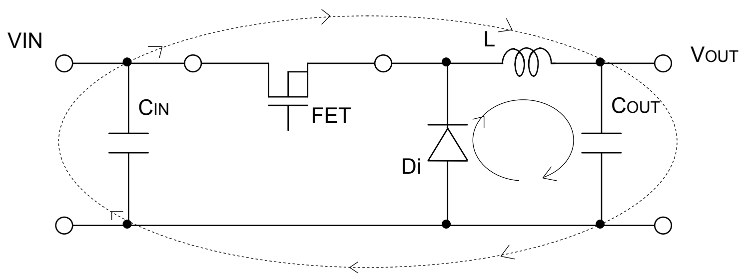


Fig.25 Current loop in Buck regulator system

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected as close as possible to the VIN terminal.
- When there is unused area on PCB, please arrange the copper foil plain of DC nodes, such as GND, VIN and VOUT for helping heat dissipation of IC or circumference parts.
- To avoid the noise influence from AC combination with the other line, keep the switching line such as SW not extend as much as possible, and trace shortly and thickly to coil.
- Keep sensitive signal traces such as trace connected FB and COMP away from SW pin.
- The inductor, the shot key diode and the output capacitors should be placed close to SW pin as much as possible.

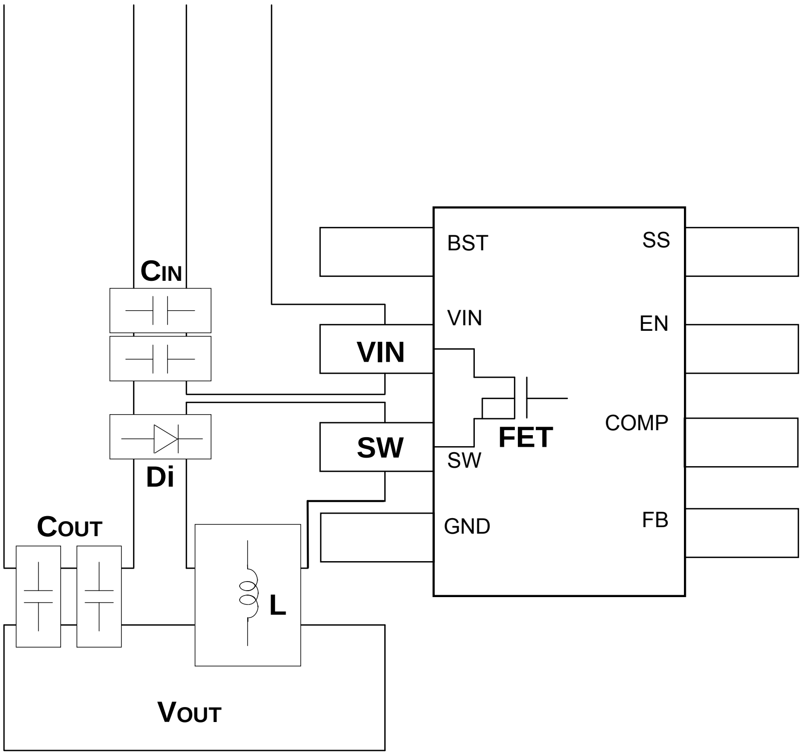


Fig.26 The example of PCB layout pattern

I/O Equivalent Circuit

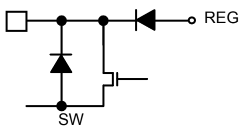
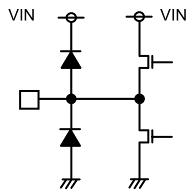
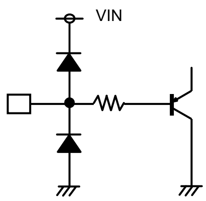
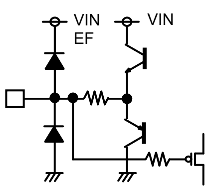
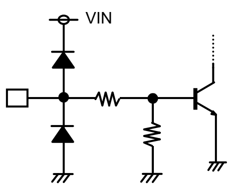
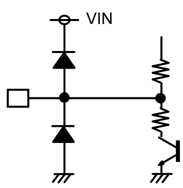
1.BST	3.SW	5.FB
		
6.COMP	**7.EN**	**8.SS**
		

Fig.27 I/O Equivalent Circuit

●Operational Notes

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig.28, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

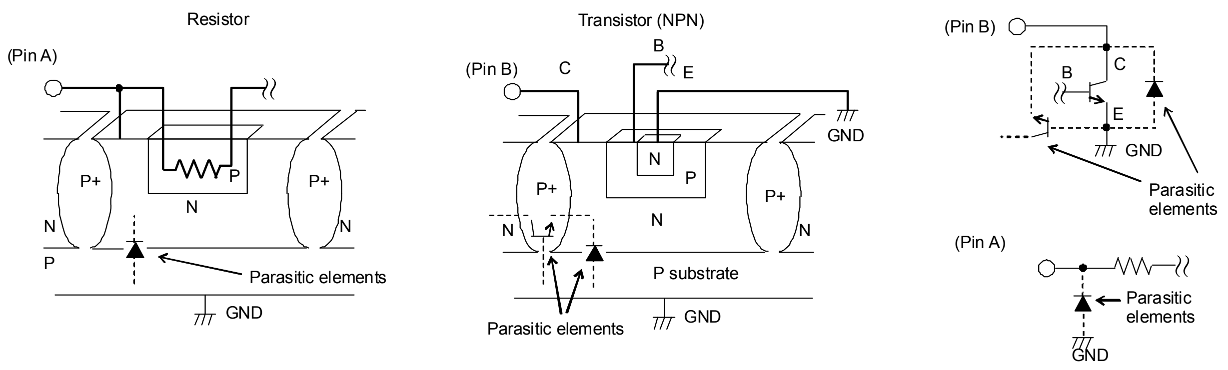


Fig.28 Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the
IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

Power Dissipation

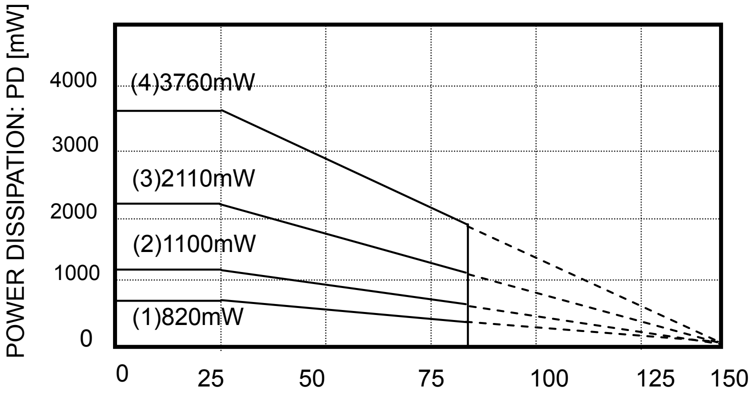


Fig.29 AMBIENT TEMPERATURE: Ta [°C]

HTSOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

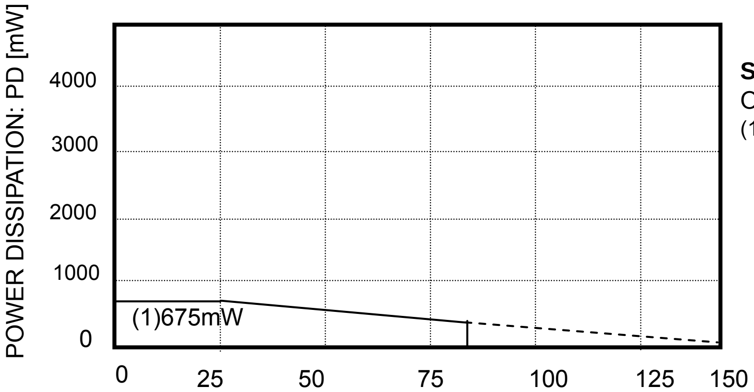
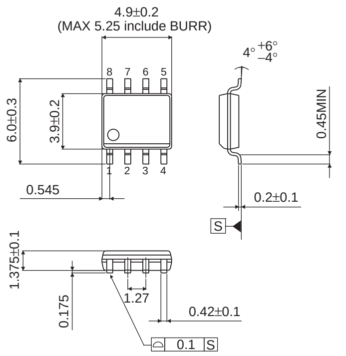


Fig.30 AMBIENT TEMPERATURE: Ta [°C]

SOP-J8 Package
On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)

●Physical Dimensions, Tape and Reel information

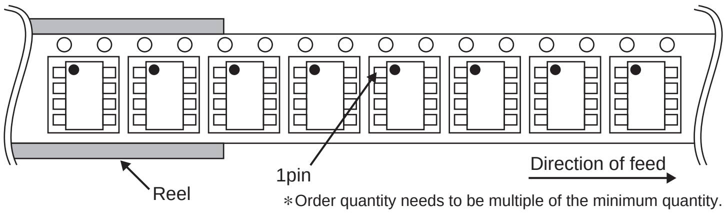
SOP-J8



(Unit : mm)

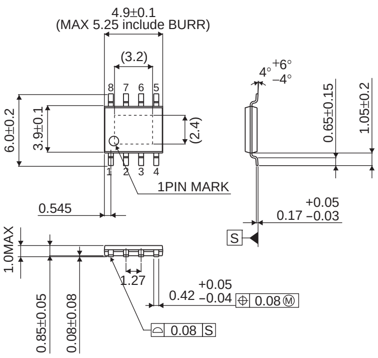
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

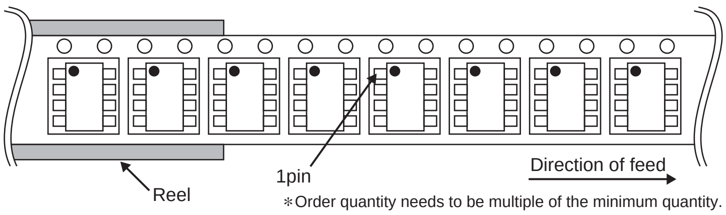
HTSOP-J8



(Unit : mm)

<Tape and Reel information>

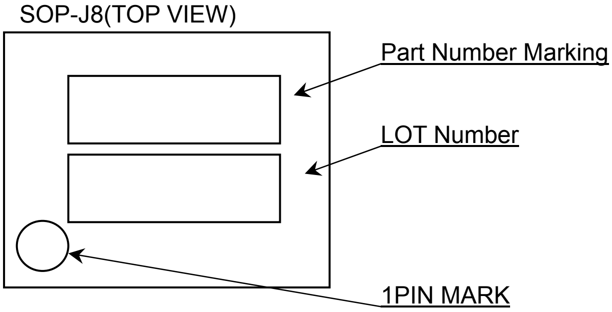
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



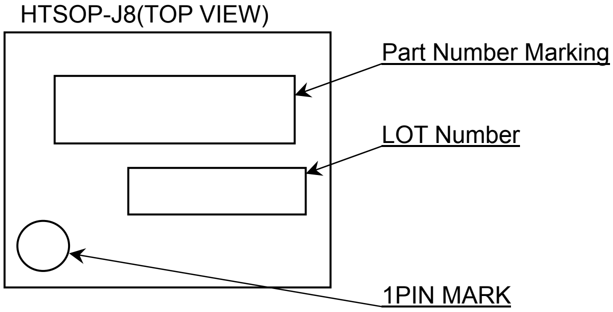
*Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams

SOP-J8(TOP VIEW)



HTSOP-J8(TOP VIEW)



Part Number Marking	Package	Orderable Part Number
D9325	SOP-J8	BD9325FJ-E2
D9326	HTSOP-J8	BD9326EFJ-E2
D9327	HTSOP-J8	BD9327EFJ-E2

●Revision History

Date	Revision	Changes
11.Apr.2012	001	New Release

Notice

●General Precaution

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

●Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

●Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

●Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

●Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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