System Power Supply for TV Series

Built-in 1ch FET Synchronous Light Load Type DC/DC Converter

BD8622EFV

No.09034EAY04

●Description

BD8622EFV has realized the high performance and reliability required as a power supply for thin-screen TV.
Due to the high-speed load response, it is most suitable for TV-purpose processors with increasingly high performance, and due to the wide phase margin it leaves a good margin for board pattern & constant setting and so facilitates its application design.
As a high-reliability design, it has various built-in protection circuits (overcurrent protection, output voltage abnormal protection, thermal protection, and off-latch function at the time of abnormality etc.), therefore as an advantage it does not easily damage in every possible abnormal condition such as all-pin short circuit test etc. and hence most suitable for thin-screen TV which requires the high reliability.

●Features

1) High efficiency in all load area
2) 3.0A output current
3) PWM mode/PFM mode switch(automatic operation)
4) Low current mode/Rorripplmord switch with terminal MODE
5) Low RDS(ON) internal switches : 75mΩ(typ.)
6) ±1% reference voltage accuracy
7) Programmable frequency : 250kHz-1MHz
   (Can the adjustment by an external synchronization and the terminal RT resistance.)
8) Terminal RT OPEN/SHORT detecting function
9) Over current protection function
10) Output over voltage/low voltage protection function (over : FB > VREF +60mV , low : FB < VREF -60mV)
11) Timer off latch function in abnormal circumstances
12) Thermal shutdown function
13) Under voltage protection
14) Soft start/start delay circuit
15) Soft start time out function
16) Protecting BUS function with terminal PDET
17) HTSSOP-B20 package

●**Electrical characteristic**

(Unless otherwise noted Ta=25°C, VIN=3.3V, GND=0V)

Parameter	Symbol	Specification value			UNIT	Condition
		MIN	TYP	MAX		
VIN supply current (operating)	I_{Q_active}	-	210	350	μA	V_{FB} = 0.83V, V_{FC} = 1V
VIN supply current (standby)	I_{Q_stby}	-	0	1	μA	V_{EN} = 0V
Reference voltage (VREF)	V_{REF}	0.792	0.8	0.808	V	
Output rise detection voltage	V_{OVP}	30	60	90	mV	Monitoring FB terminal
Output decrease detection voltage	V_{LVP}	-90	-60	-30	mV	Monitoring FB terminal
Terminal PDET output current	I_{PDET}	0.4	-	-	mA	V_{PDET}< 0.3V
Oscillation frequency	f_{OSC}	500	550	600	kHz	R_{RT}= 220kΩ
Pch FET ON resistance	R_{PFET}	-	75	110	mΩ	I_{SW} = 1A
UVLO voltage	V_{UVLO}	2.35	2.50	2.65	V	
SW leak current	I_{LSW}	-	0	1	μA	V_{EN}= 0V, V_{IN} = 5.5V
EN terminal H threshold voltage	V_{ENH}	1.1	-	-	V	
EN terminal L threshold voltage	V_{ENL}	-	-	0.4	V	
FC sink current	I_{FCSI}	10	20	-	μA	
FC source current	I_{FCSO}	-	-20	-10	μA	
SS/DELAY terminal source current	I_{SSSO}	2	4	6	μA	
Terminal PDET pull-up resistor	R_{PDET}	100	170	250	kΩ	

V_{FB}:FB terminal voltage, V_{EN}:EN terminal voltage, V_{FC}:FC terminal voltage, V_{PDET}: PDET terminal voltage

Current capability should not exceed Pd.

●Block Diagram

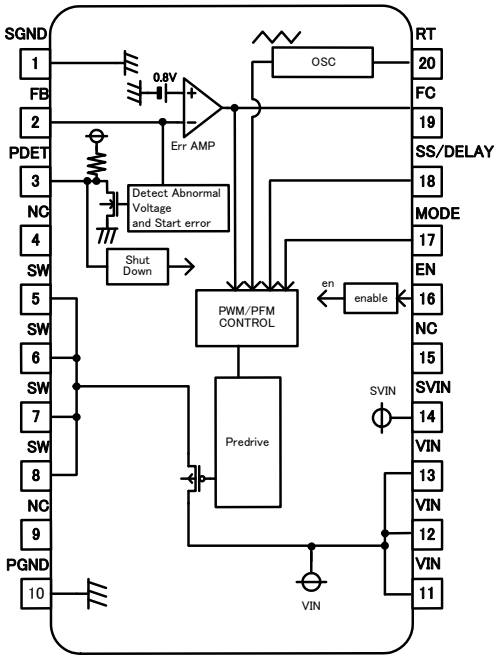
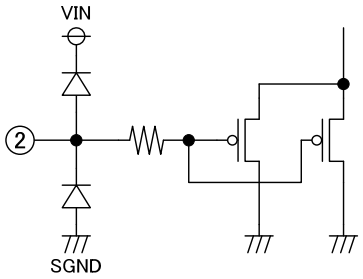
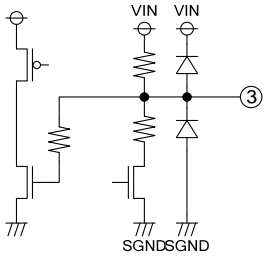
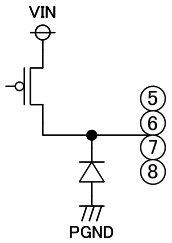


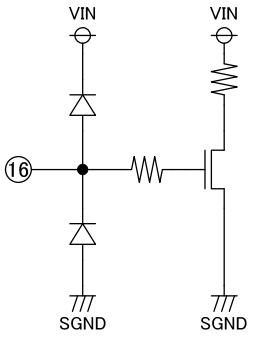
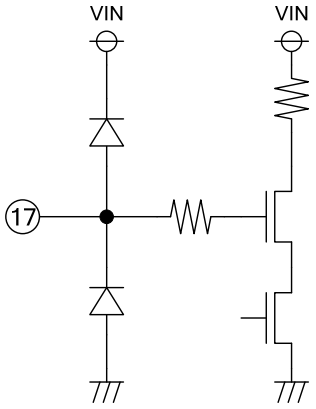
Fig1 Block diagram

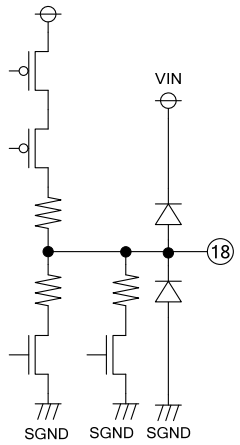
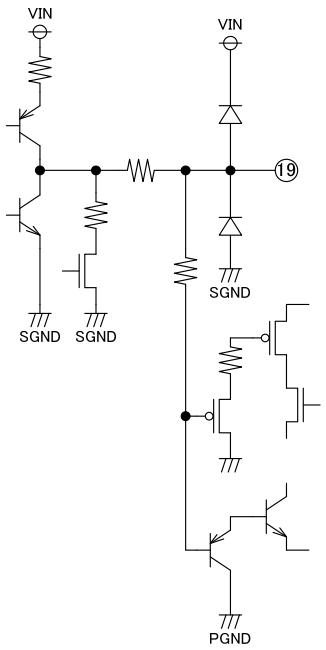
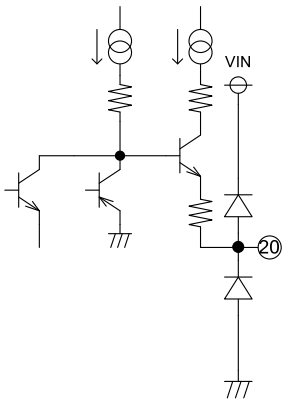
●Pin Description

No.	Symbol	Description	Explanation
1	SGND	Signal GND terminal	Small signal system GND
2	FB	Feed back terminal	Output voltage detection
3	PDET	Abnormal state notification and external IC abnormality detection terminal	Protecting BUS communication terminal
4	NC		
5	SW	Switching output terminal	
6	SW		
7	SW		
8	SW		
9	NC		
10	PGND	Power GND terminal	GND for power MOSFET
11	VIN	Power supply input terminal	Power supply input. The decoupling is done to PGND
12	VIN		
13	VIN		
14	VIN		
15	NC		
16	EN	Enable input	ON/OFF control for device operation
17	MODE	MODE selection terminal	The operation mode is switched according to the input voltageat a light load.
18	SS/DELAY	Soft start adjustment capacity connection terminal	The soft start time is adjusted with the connected capacitor
19	FC	Error amplifier output	Error amplifier phase compensation point
20	RT	Frequency adjustment resistance connection terminal	The switching frequency is set by the connected resistance

● **Pin equivalence circuit diagram**

No.	Symbol	Explanation	Terminal equivalent circuit diagram
1	SGND	GND (connected 0V)	
2	FB	Output voltage detection terminal	
3	PDET	Protecting BUS I/O terminal	
5,6,7,8	SW	Output terminal	
10	PGND	Power GND (Same voltage as SGND)	
11,12,13	PVIN	Power supply input terminal	
14	SVIN	Power supply input terminal	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
16	EN	Enable terminal	
17	MODE	Operation mode switch terminal at light load	

No.	Symbol	Explanation	Terminal equivalent circuit diagram
18	SS /DELAY	Soft start time adjustment terminal	
19	FC	Error amplifier compensation terminal	
20	RT	Oscillator frequency adjustment terminal	

●Operation description

Enable control

The device can be controlled ON/OFF by EN terminal (16 pin) voltage.

An internal circuit starts when VEN reaches 1.1V.

When standing up of VIN is too steep (1msec or less), a defective start might be caused according to the state of Pascon between GND substrate pattern and power supply–when the terminal EN is short–circuited to the terminal VIN and it is used.

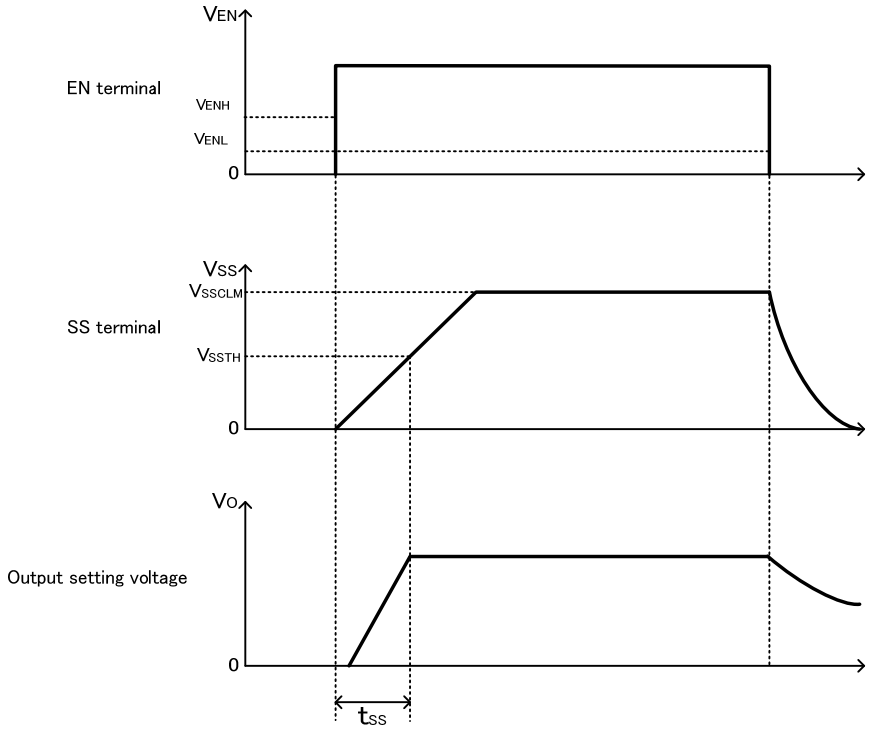


Fig.2 ON/OFF transition wave form in EN controlling

Soft start time set function

As for BD8622EFV, output can do soft start without overshoot by charging soft start capacity (CSS) connected between SS and SGND terminal.

Also, soft start time (tss) can be set by setting soft start capacity (CSS) arbitrarily.

OSC oscillation frequency setting function

The output oscillation frequency can be set by connecting resistance between terminal RT (20 pins) and SGND (range = 250kHz - 1MHz)

The relation between RT terminal resistance and the oscillation frequency follows Fig.3.

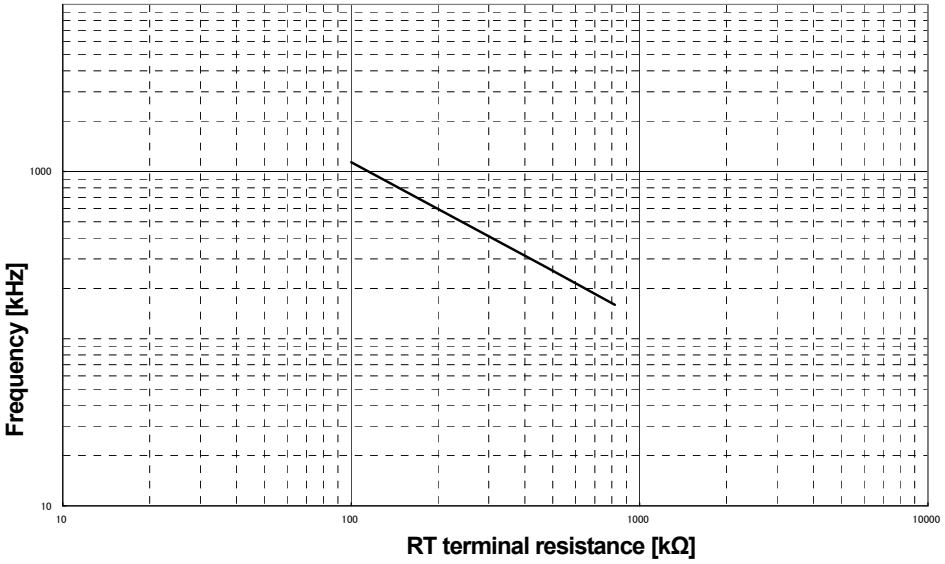


Fig.3 RT resistance-oscillation frequency

Light load mode operation

・Low current mode

When the terminal MODE (17 pins) is made "H", low current mode operation becomes effective. The characteristic of the efficiency valuing is obtained in low current mode operation at a light load.

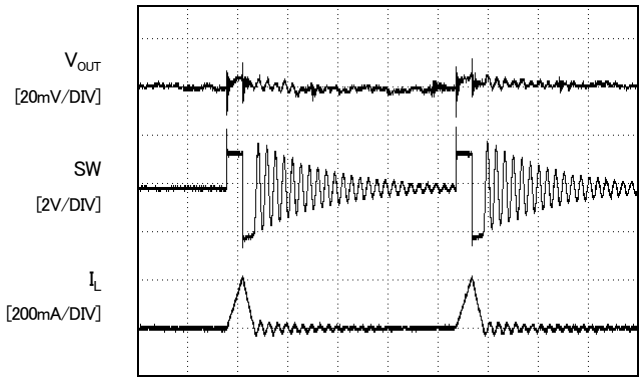


Fig.4 Low current mode operation

・Low ripple mode

When the terminal MODE is made "L", the Low ripple mode operation becomes effective. It becomes operation of valuing a low ripple in the Low ripple mode operation at a light load.

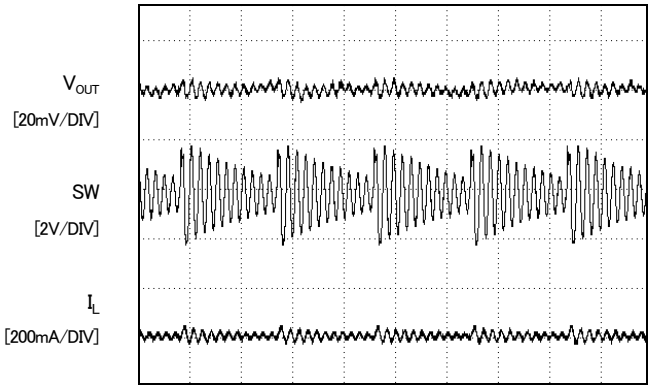


Fig.5 Low ripplemord operation

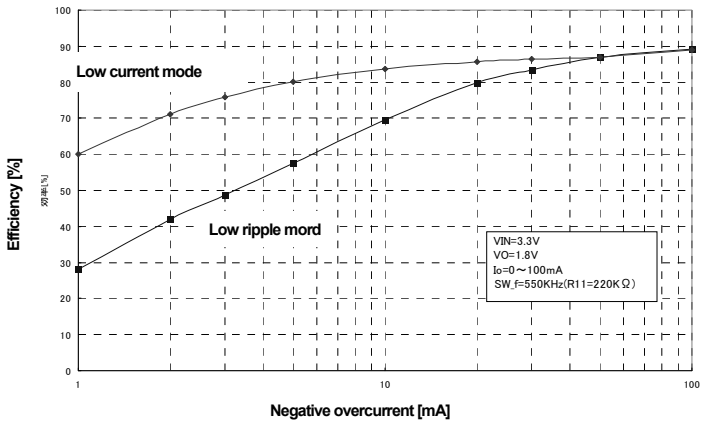


Fig6 Light load mode efficiency comparison

● **Protection function**

Protection circuit is effective for destruction prevention due to accident so that avoid using under continuous protection operation.

Low voltage protection function (LVP)

The voltage of the terminal FB (2 pins) is compared with internal reference voltage VREF.

If FB terminal voltage falls below V_{LVP}(= VREF -60mV) and the state continues for 500us, output changes to low voltage and the state is fixed. In that case , PDET (3pin) output changes to L.

Table 1 output low voltage protection function

EN terminal	SS terminal	FB terminal	Low voltage protection function	Low voltage protection operation
$>V_{ENH}$	>1.4V(typ)	$<V_{LVP}$	Effective	ON
		$>V_{LVP}$		OFF
	<1.4V(typ)	–	Invalidity	OFF
$<V_{ENL}$	–	–	Invalidity	OFF

＊ Low voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

Over voltage protection function(OVP)

The voltage of the terminal FB is compared with internal reference voltage VREF.

If FB terminal voltage is over Vovp (=VREF +60mV) and the state is continues for 500usec, output changes to low voltage and the state is fixed.

Table 2 output overvoltage protection function

EN terminal	SS terminal	FB terminal	Over voltage protection function	Over voltage protection operation
$>V_{ENH}$	>1.4V(typ)	$>V_{OVP}$	Effective	ON
		$<V_{OVP}$		OFF
	<1.4V(typ)	–	Invalidity	OFF
$<V_{ENL}$	–	–	Invalidity	OFF

＊ Over voltage protection function is available when SS terminal voltage becomes more than 1.4V (typ) in the transition to ON control (during soft start).

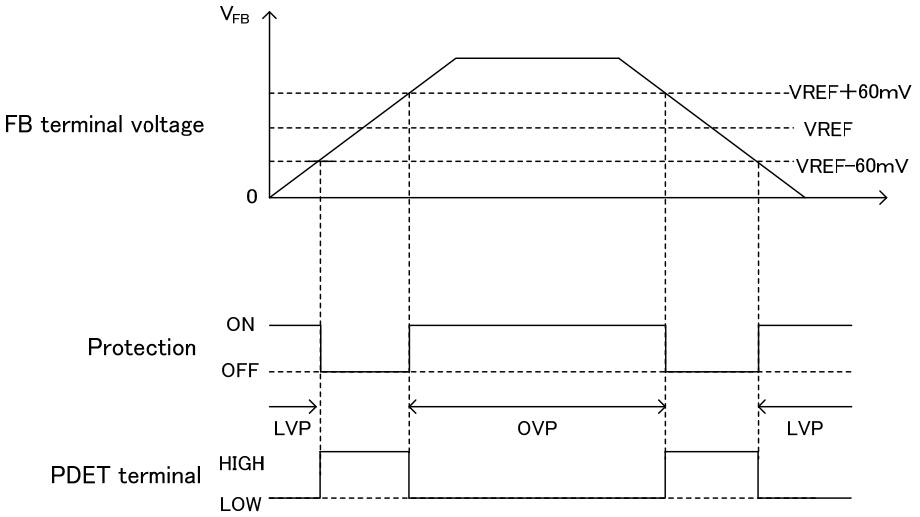


Fig.7 Output voltage error detection range

Under voltage lock out protection (UVLO)

As for BD8622EFV, the power-supply voltage decrease detection protection circuit is built in.
It the input voltage decrease below the UVLO voltage (2.5V typ), the device state changes to the standby mode (Moreover, to prevent the chattering of the output) hysteresis width of 100mV(typ) has been installed in the UVLO cancel voltage.

RT terminal open/short protection function (RTO/RTS)

RT terminal opening/short protection function prevent the clock from abnormal oscillation.
If RT terminal open/short protection function is detected, output voltage changes to low level and is fixed.

Terminal RT opening/short protection function is available if the state continue for 500usec, abnormal detection operates when the state continues about 500μsec(typ).

Soft start time-out function

If VSS doesn't exceed VSSTH within 64msec (typ) since a soft start began, BD8622EFV controls an off latch.
Vo is fixed in a low level.

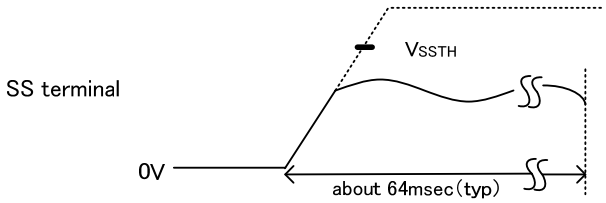


Fig.8 Soft start time-out

Thermal shut down function

Thermal shut down circuit (TSD circuit) is built into BD8622EFV. When the temperature of the chip exceeds Tjmax=175, the DC/DC converter is fixed in a low voltage.
TSD function is aimed to shut down IC from thermal reckless driving under an abnormal state to exceed Tjmax=175.
It aims at neither protection nor the guarantee of the set. Therefore, please do not use this function to protect the set.

Over current protection function

The over current protection function has been achieved by limiting the current that flows on high side MOSFET.
The current is controlled in every one cycle of the switching frequency. When an abnormal state continues for about 500μsec(typ), the output is fixed in a low level.

Protecting BUS function with terminal PDET

The terminal PDET (3 pins) monitors whether IC is normal or not. When IC becomes abnormal, the PDET output is reduced at "L" level with the output voltage fixed “L” level at the same time. Moreover, it is possible to make the output fix in a low level by compulsorily reducing the terminal PDET at "L" level from the outside.

When two or more BD8622EFV is used in the application, this function prevents the IC from destroying, because one IC error transmits all other ICs by PDET line in the condition that PDET terminals are connected each other.

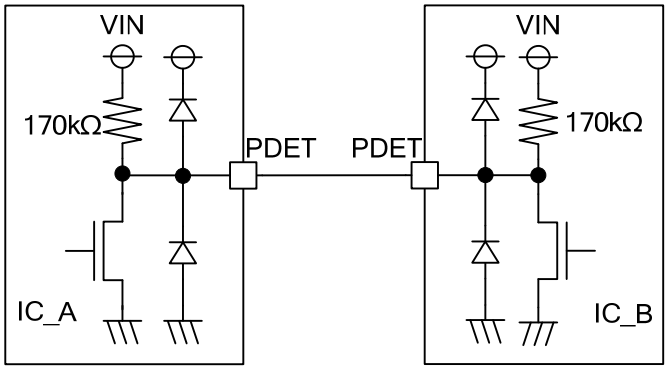


Fig.9 Protecting BUS communication

※Please give the terminal PDET as OPEN when you do not use protecting BUS function.

Error detection (off latch) release method

BD8622EFV enters the state of an off latch when the protection function operates.

To release the off latch state, EN terminal voltage should be changed to low level once time.

● **Each characteristic reference data**

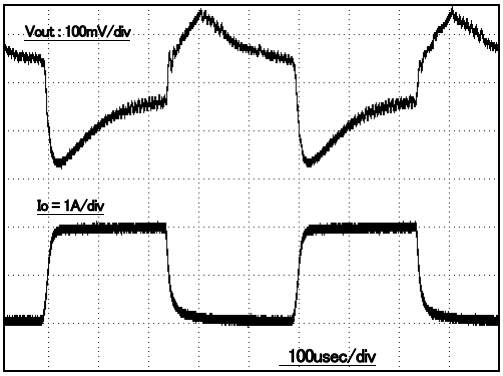


Fig.10 Output load response

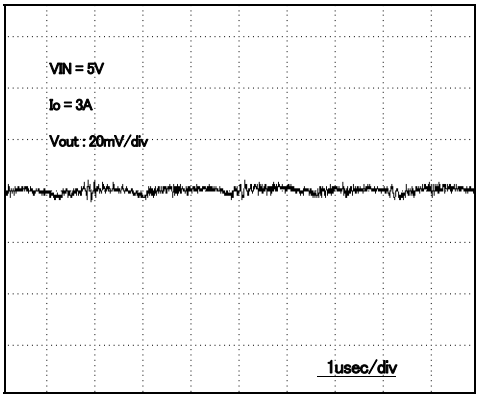


Fig.11 Output ripple

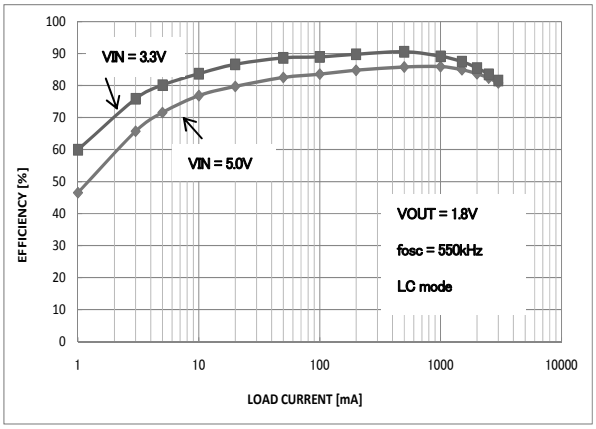


Fig.12 Efficiency

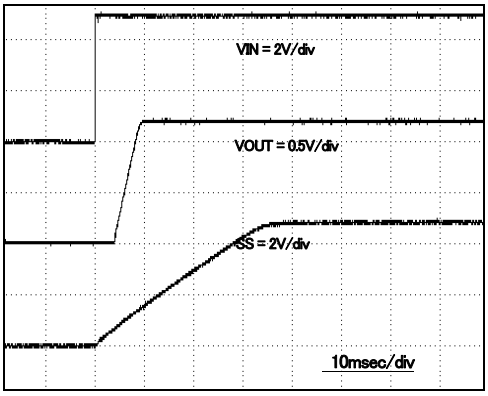


Fig.13 Soft start

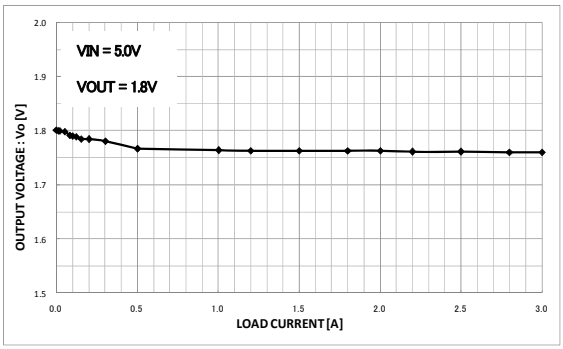


Fig.14 Regulation

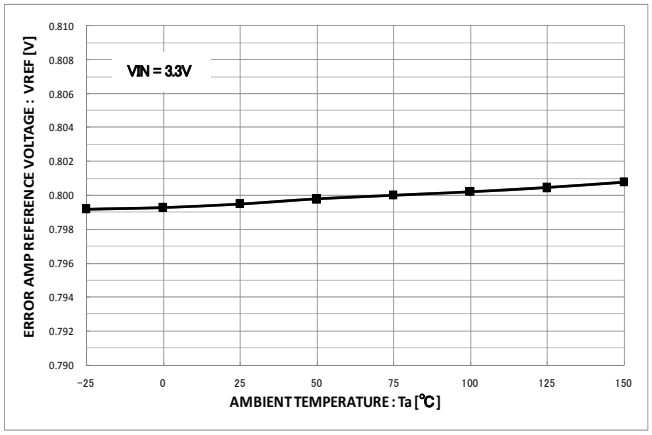


Fig.15 Reference voltage - Temperature characteristic

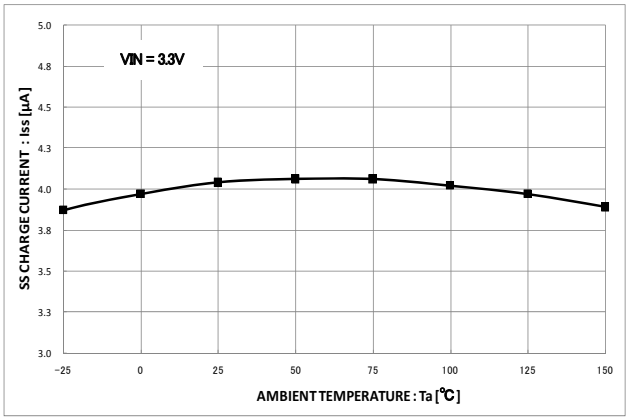


Fig.16 SS Charging current - Temperature characteristic

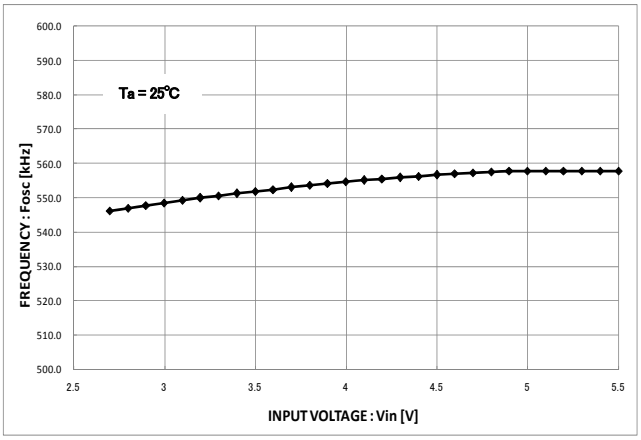


Fig.17 Switching frequency-power-supply voltage characteristic

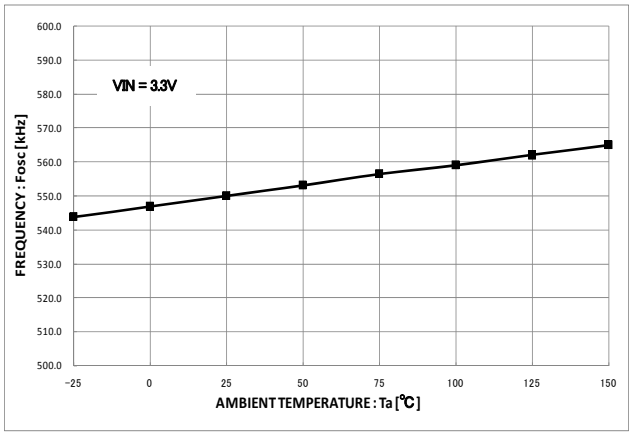


Fig.18 Switching frequency-temperature characteristic

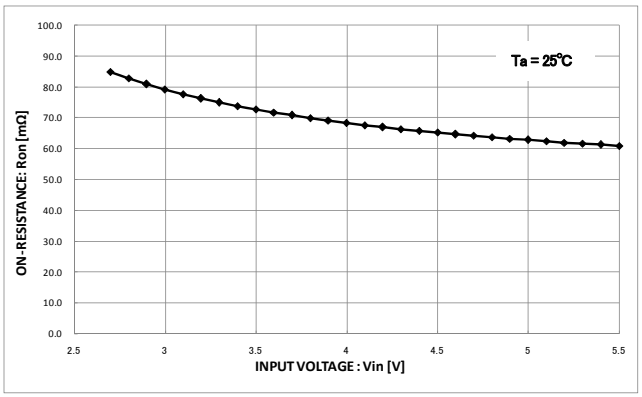


Fig.19 PMOS on resistance-power-supply voltage

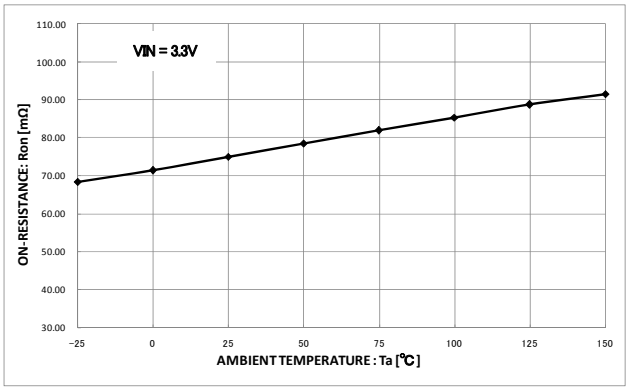


Fig.20 PMOS on resistance-temperature characteristic

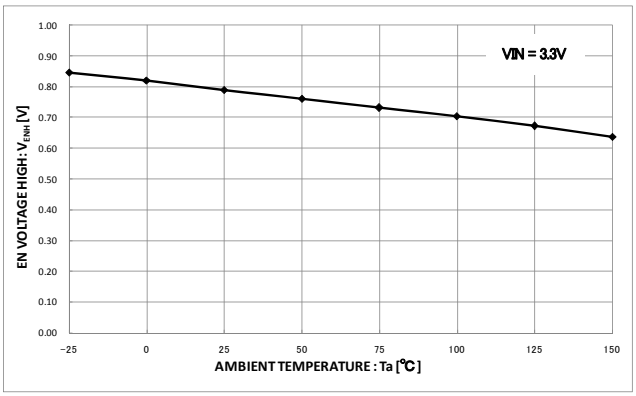


Fig.21 Terminal EN H voltage-temperature characteristic

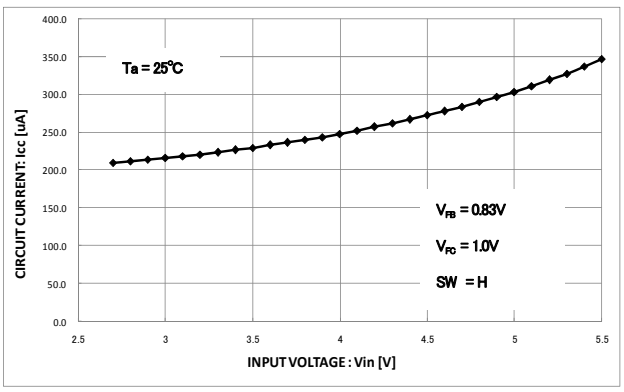


Fig.22 Circuit current-power-supply voltage characteristic

● **External parts setting method**

Output voltage setting method

The output voltage can be arbitrarily set by external resistance.

$$Vo = \frac{(R1+R2)}{R2} VREF$$

Please select the constant of R1 and R2 by this expression.

Please select the current that flows to R1 and R2 to become much smaller than output current.

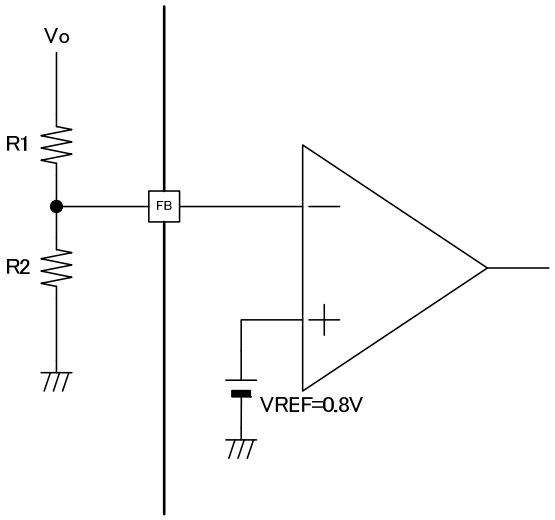


Fig.23 Output voltage setting circuit

Soft start time setting method

BD8622EFV can soft start without overshoot because of a charge current to the soft start capacitance (CSS).

The soft start time can be set by connecting soft start capacity (CSS).

When the EN terminal voltage is set VIH_EN or more, the charge to the capacity between SS/DELAY and SGND terminal is begun. The output voltage becomes soft start in proportion to a SS/DELAY terminal voltage rising. When the SS/DELAY terminal voltage exceeds VSSTH, the output voltage is fixed in a setting value.

Please set soft start time (tss) in 1msec-30msec.

$$t_{SS} = \frac{V_{SSTH} \times C_{SS}}{I_{SS}}$$

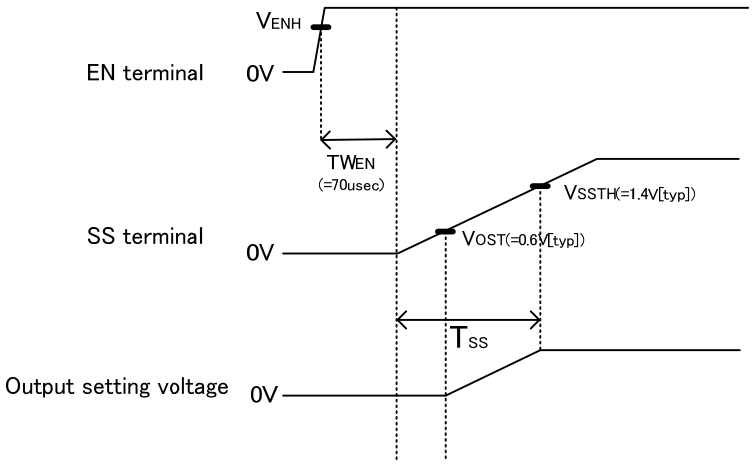


Fig.24Soft start

Selection of inductor (L)

Please select the value of the inductor according to the following expressions.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} [H]$$

(⊿ IL: Output ripple current , f: Switching frequency)

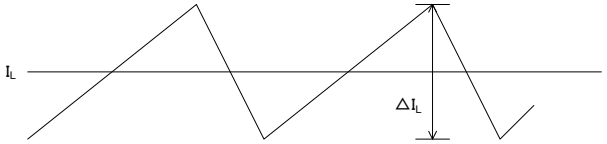


Fig.25 Current of output ripple

Please have and select an enough margin so that the current peak should not exceed the ratings current value of the inductor.

Selection of input capacitor (Cin)

Please use a low ESR input capacitor which can be used with high voltage and ripple current to prevent a big transition voltage.

Selection of diode

Please have and set the margin enough to the current rating of the diode for the maximum load current.
Moreover, please similarly have and set the margin enough to a ratings reverse-voltage for the maximum input voltage.

Phase compensation circuit setting method

The phase margin can be set by connecting capacity and resistance between the terminal FC and the terminal SGND.
Please set the zero crossing frequency (The 0dB gain's frequency) to about 1/10 or less of the switching frequencies.
When the stability level of the loop system is low, the phase room is improved by setting 0 crossing low.
It lowers when 0 crossing frequency rises when C1 is greatly reduced, and R1 is set oppositely.
Please connect the capacitor of about 47pF with C2 for the high frequency noise absorption.

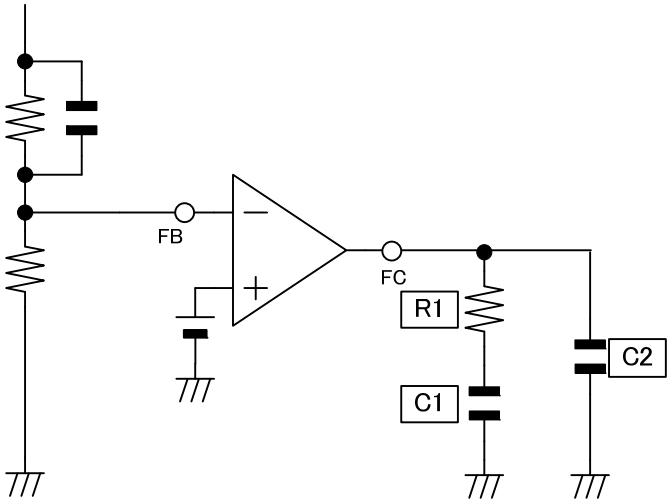


Fig.26 Phase amends part external circuit chart

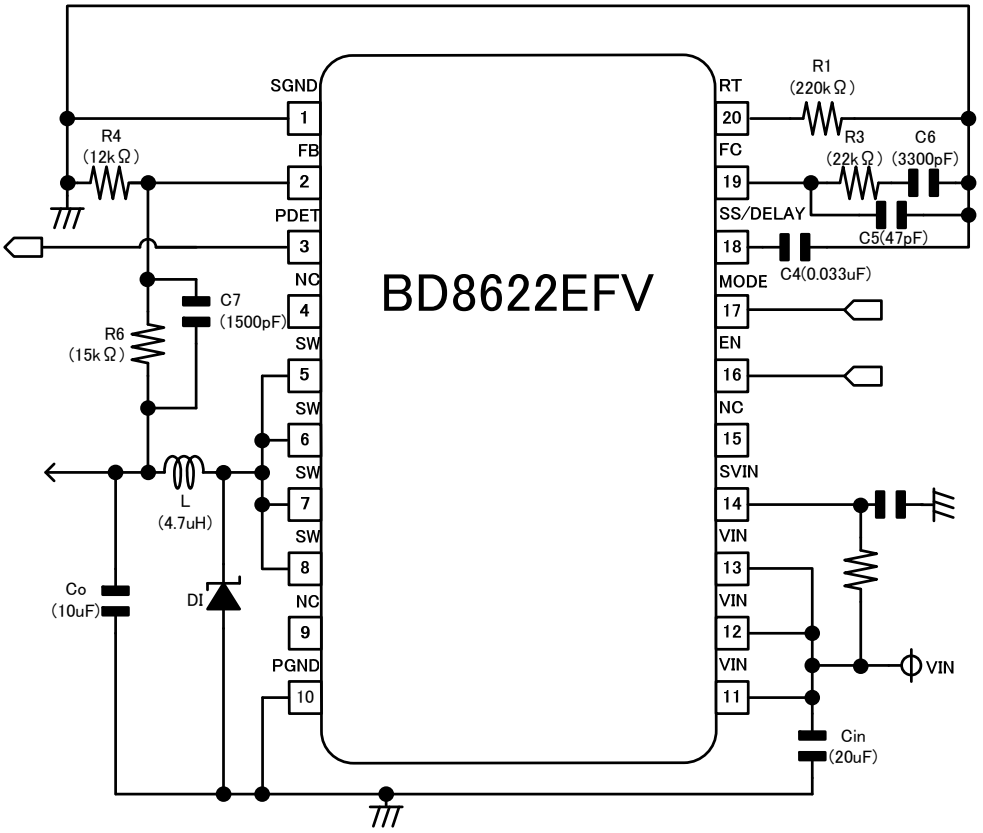
● **Typical application**

【Condition】

VIN = 5.0V

VOUT = 1.8V

fosc = 550kHz （R_RT = 220kΩ）



Inductor ： SLF7055T-4R7N (TDK)

Diode ： RB051L-40 (ROHM)

POSCAP ： 4TPE150MAUB (SANYO)

Fig.27 Typical application

Notes

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