

●A TABLE OF CONTENTS

1.What is Op-Amp/Comparator?

- 1.1 Model of amplifier (Voltage amplifier) and Op-Amp
- 1.2 What is Op-amp/Comparator?
- 1.3 Op-amp and Comparator circuit construction

2.Absolute maximum rating

- 2.1 Rated power supply voltage
- 2.2 Rated differential input voltage
- 2.3 Rated common mode input voltage
- 2.4 Maximum power dissipation and storage temperature range
- 2.5 Electrostatic discharge tolerance

3.Electrical characteristic of op-amp and comparator

- 3.1 Circuit current/quiescent current I_{cc} / I_q and power consumption
- 3.2 Input offset voltage V_{io}
- 3.3 Input bias current/Input offset current I_b/I_{io}
- 3.4 Common mode input voltage range V_{icm}/CMR
- 3.5 Maximum output voltage (output voltage range) V_{om} / V_{oh} , V_{ol}
- 3.6 Common Mode Rejection Ratio (CMRR)
- 3.7 Power Supply Rejection Ratio (PSRR)
- 3.8 Large signal voltage gain (Large amplitude voltage gain, open loop voltage gain) A_v
- 3.9 Slew Rate (SR)
- 3.10 Response time t_{re} / t_{pHL} / t_{pLH}
- 3.11 Open loop voltage gain frequency characteristics and unity gain frequency/gain bandwidth product
- 3.12 Model of negative feedback system and oscillation condition
- 3.13 Total Harmonic Distortion plus Noise (THD + N)
- 3.14 Equivalent input noise source

●1.What is Op-Amp/Comparator?

1.1 Model of amplifier (voltage amplifier) and Op-Amp

An amplifier has a function to increase an input signal by amplification factor of amplifier for outputting. Electric / Electronic circuit uses voltage and current in the main for input signal and output signal. Configuration of such amplifying circuit is classified into the four types shown below:

1. VCVS (Voltage Controlled Voltage Source) Voltage input/Voltage output
2. CCCS (Current Controlled Current Source) Current input/Current output
3. VCCS (Voltage Controlled Current Source) Voltage input/Current output
4. CCVS (Current Controlled Voltage Source) Current input/Voltage output

Function required for all four types shown above is to detect and amplify an input signal without attenuating, and supply output signal with no attenuation of the load. We will consider the function required for an amplifier by modeling the input signal source, amplifier, and load. Figure 1.1.1 (a) - (d) show the model of four amplifiers described above including the input signal source and load. Figure 1.1.1 (a) shows the model of voltage controlled voltage source. Input resistance of this amplifier is represented by R_i , output resistance by R_o , and amplification factor by A_v . Input signal source is modeled by voltage source V_s , output resistance R_s , and load R_L . Output voltage is calculated by the equation below by use of these models:

$$V_o = (R_L / (R_o + R_L)) \cdot A_v \cdot (R_i / (R_s + R_i)) \cdot V_s \tag{1.1.1}$$

Signal voltage is divided by R_s and R_i , so that the attenuated signal is input to the amplifier.

Output voltage from the amplifier is divided by R_o and R_L , and supplied to the load.

The greater R_i is, the less attenuated is the signal voltage input to the amplifier; the smaller R_o is, the less attenuated is the output voltage supplied to the load.

Assume that $R_i = \infty [\Omega]$ and $R_o = 0 [\Omega]$ in the formula (1.1.1), then

$$V_o = A_v \cdot V_s \tag{1.1.2}$$

We understand that amplified voltage can be supplied to the load without attenuating, with no attenuation of voltage at the signal source. Therefore, it is desirable that infinite input resistance and zero output resistance are provided for voltage controlled voltage source. Input resistance and output resistance required for the amplifier of the other three types are summarized in the table 1.1.1. Op-amp is a voltage controlled voltage source when classified into the four types of amplifier described above. Therefore, high input resistance and low output resistance are preferable for an op-amp, which in general has a circuit configuration close to such characteristics.

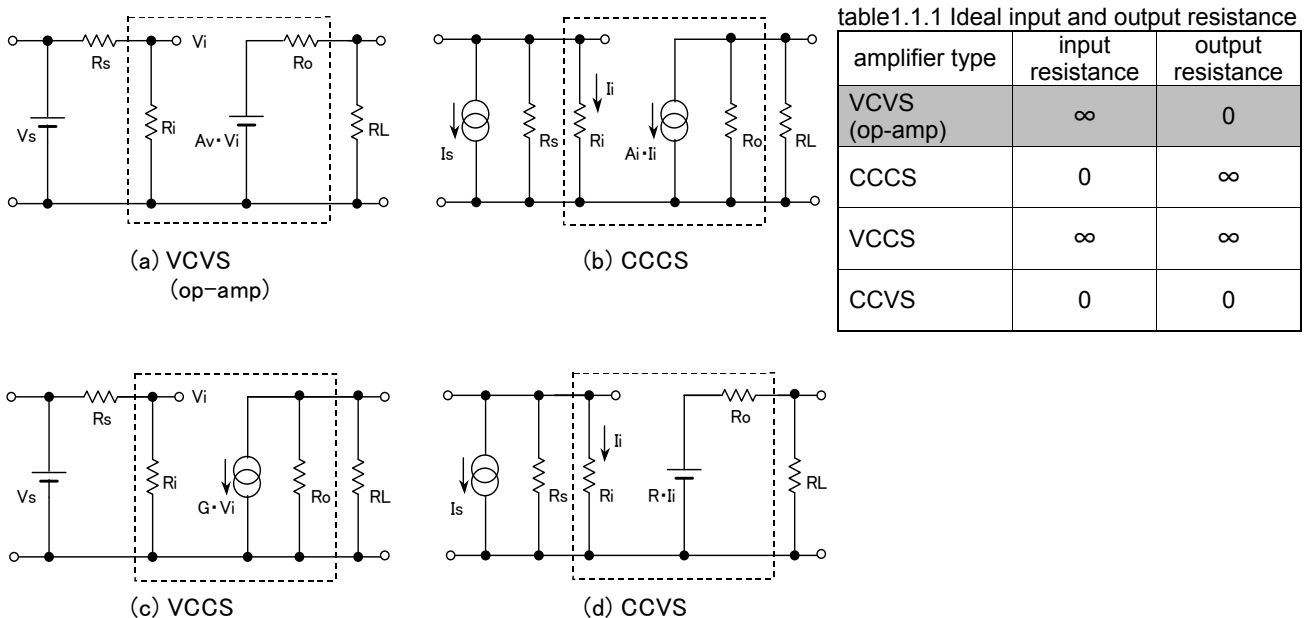


Fig.1.1.1 The type of amplifier

1.2 What is Op-amp/Comparator?

Op-amp (operational amplifier) is a differential amplifier provided with high input resistance and low output resistance. It consists of + input terminal (non-inverting input terminal), - input terminal (inverting input terminal), output terminal and power supply terminal (plus and minus side), and the differential voltage between + input terminal and - input terminal is increased by the amplification factor provided by the amplifier, and output.

Drawing symbol of op-amp is shown in figure 1.2.1.

Op-amp, in general use, composes a negative feedback circuit by connecting resistors and capacitors between the output terminal and - input terminal, and executes analogue signal processing such as amplifying of signal, addition, subtraction, and filtering. Figure 1.2.2 shows an example of use for an amplifier. This circuit, which is called an inverting amplifier, increases an input signal by an amplification factor determined by resistance R1 and R2, and outputs a signal with phase reversed 180 degrees. When the amplification factor of op-amp is assumed to be "a", input signal "Vin", and output signal "Vout", "Vout" can be represented by the equation below:

$$V_{out} = -(R_2 / (R_1 + (R_1 + R_2) / a)) \cdot V_{in} \tag{1.2.1}$$

Amplification factor of op-amp (voltage gain) is great in general. Therefore the equation is approximated as follows:

$$V_{out} \approx -(R_2 / R_1) \cdot V_{in} \tag{1.2.2}$$

High amplification factor is desired for op-amp in order to make output voltage error due to amplification factor as small as possible. When we review the fact that the amplification is great, it means that the potential difference between + input terminal and - input terminal is made as small as possible. In other words, the greater the amplification factor is, the more established is the relation $V_{in+} = V_{in-}$. This relation where potential of + input terminal is almost equal to potential of - input terminal is called virtual short-circuit. When negative feedback circuit is configured in use, this relation is established, and application circuit is designed by use of this relation.

Terminal of comparator consists of + input terminal, - input terminal, output terminal, and plus/minus power supply terminal, which is the same as op-amp. Drawing symbol is also the same as op-amp (figure 1.2.1). It provides a circuit which amplifies the potential difference between two input terminals and outputs either high or low. It is used in general for a voltage comparator circuit for fixing the potential of either + input terminal or - input terminal, and determining the high or low level of voltage of input signal with reference to such potential.

The output voltage level is as follows:

When "Potential of + input terminal > Potential of - input terminal" is established, high level is output.

When "Potential of - input terminal > Potential of + input terminal" is established, low level is output.

Great difference between the op-amp and comparator is the availability of phase compensation capacitor. Op-amp requires phase compensation capacitor for preventing oscillation because it configures a negative feedback circuit in use, while comparator does not require this capacitor because it does not configure negative feedback. Phase compensation capacitor limits the response time of input/output time. Comparator which has no phase compensation capacitor has a greatly improved response capability in comparison with op-amp.

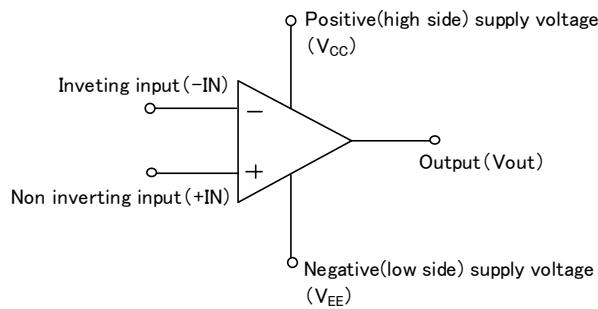
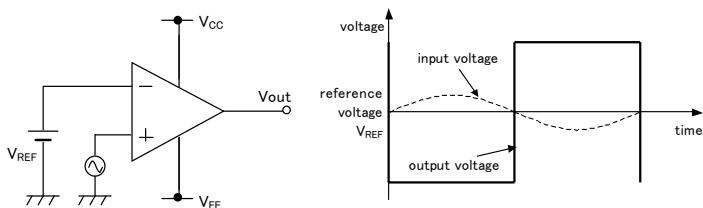
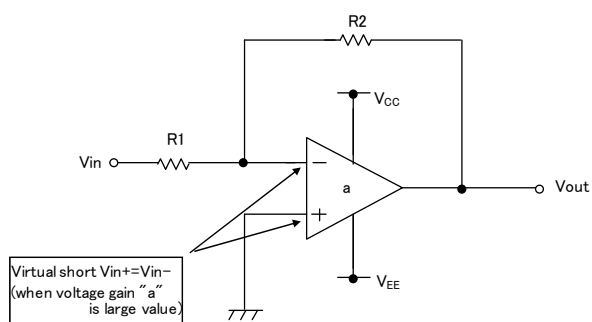
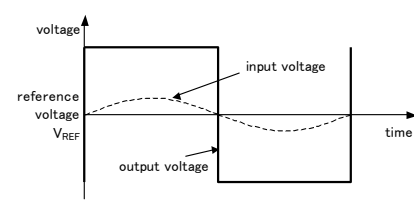
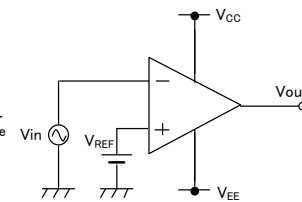
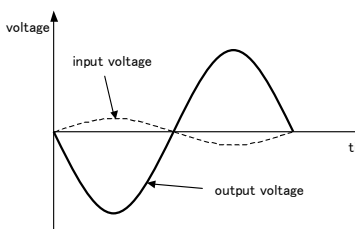


Fig.1.2.1. Op-amp and Comparator symbol



(a) non inverting voltage comparator

Relationship of input and output voltage
 $V_{out} = a \cdot (V_p - V_n)$
 $(V_{in} - V_n) / R_1 = (V_n - V_{out}) / R_2$
 Equation of Output voltage
 $V_{out} = -[R_2 / (R_1 + (R_1 + R_2) / a)] \cdot V_{in}$
 $\approx - (R_2 / R_1) \cdot V_{in} \quad (A \rightarrow \infty)$



(b) inverting voltage comparator

Fig 1.2.2 inverting amplifier

Fig 1.2.3 input and output waveform of voltage comparator

1.3 Circuit construction of operational amplifier and voltage comparator

Fig 1.3.1 shows internal circuit blocks of op-amp. Basically, it is constructed by three stages, that is input stage, gain stage and output stage.

The input stage is differential amplifier that amplifies difference of two input voltage and suppress common mode voltage. Input common mode voltage range is mainly decided by this input stage.

Voltage gain of op-amp is increased by gain stage, because only input stage voltage gain is not enough.

For general op-amp, phase compensation capacitor is inserted between input and output of gain stage.

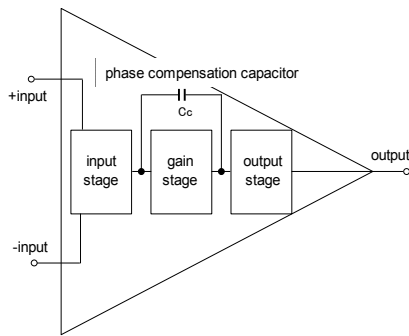
Output stage suppresses op-amp characteristic fluctuation caused by load. Output current driving ability is decided by output stage. The kinds of output circuit constructions are class A, class AB, class B, class C, and class AB etc. Harmonic distortion is deteriorated in class A, class AB, class B, class C sequence. Fig.1.3.1(b) specifies BA4558 simplified schematic. It has class AB output stages that ensure low distortion.

Fig.1.3.2 shows voltage comparator construction. That is almost same as op-amp, but it is not inserted phase compensation capacitor because applications using negative feedback are not assume.

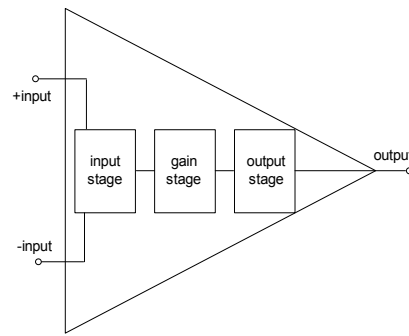
Phase compensation capacitor limits operating speed, response time is very short by rejected this capacitor.

Output stage constructions of voltage comparator are mainly open collector (or open drain) type and push-pull type.

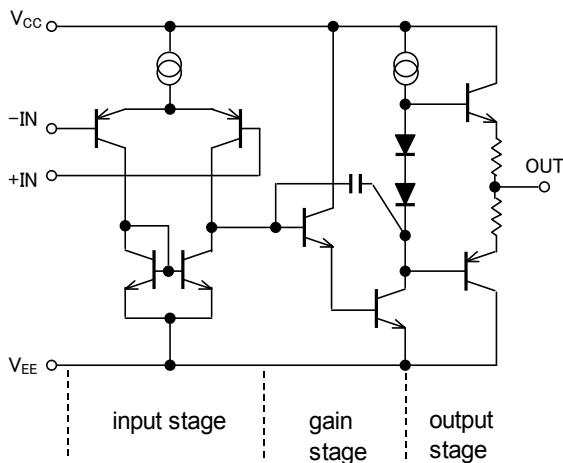
Fig.1.3.2 (b) shows BA10393 simplified schematic. The output stage is open collector type.



(a) basic op-amp building blocks

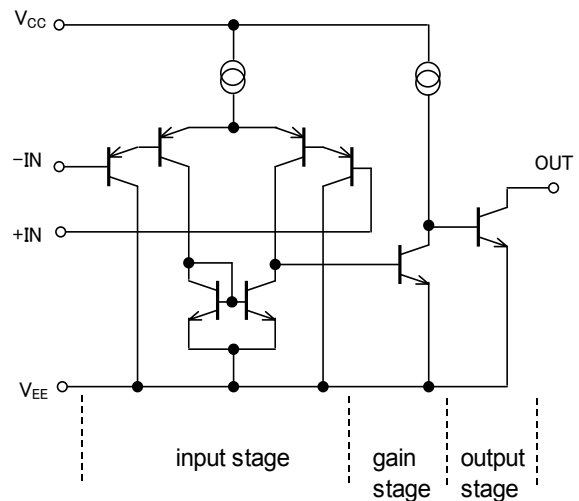


(a) basic voltage comparator building blocks



(b) BA4558 simplified schematic

Fig 1.3.1 op-amp circuit construction



(b) BA10393 simplified schematic

Fig 1.3.2 voltage comparator circuit construction

●2. Absolute maximum rating

Typical items of absolute maximum rating op-amp/comparator include the following:

1. Rated power supply voltage
2. Rated differential input voltage
3. Rated common mode input voltage
4. Storage temperature range
5. Maximum power dissipation

Absolute maximum rating refers to a condition which must not be exceeded even momentarily for the items described on specification including the above. Applying a voltage in excess of absolute maximum rating and using under high and low temperature environment may cause characteristic deterioration and destruction of IC.

2.1 Rated power supply voltage

It is the maximum power supply voltage that can be applied between plus power supply terminal (V_{CC} terminal) and minus power supply terminal (V_{EE} terminal) without characteristic deterioration and destruction of internal circuit.

Figure 2.1.1 shows an example of power supply voltage that can be applied to op-amp/comparator with rated power supply voltage 36V. Rated power supply voltage indicates the voltage between V_{CC} terminal and V_{EE} terminal, and if ($V_{CC} - V_{EE}$) does not exceed rated voltage, no problem is found in applying such voltage. Therefore, when 24[V] is applied to V_{CC} terminal and -12[V] to V_{EE} terminal, characteristic deterioration and destruction are not found. What should be noted is that rated power supply voltage and operational power supply voltage are different parameters.

Rated power supply voltage refers to a power voltage that can be applied without characteristic deterioration or destruction of IC, and does not mean a power supply voltage for normal operation. Voltage must be set within operational power supply voltage range for operating IC normally. Value of rated power supply voltage and operational power supply voltage depends on a model. They may be equal in some cases, and they may be different in other cases.

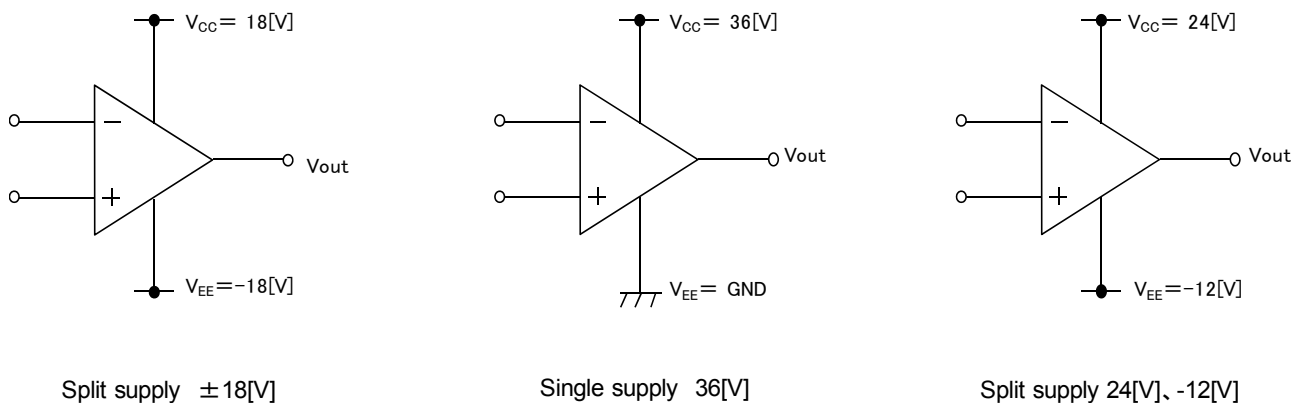


Fig. 2.1.1 Applicable supply voltage
(In case of rated supply voltage is 36V)

2.2 Rated differential input voltage

It refers to the maximum voltage that can be applied between + input terminal (non-inverting input terminal) and - input terminal (inverting input terminal) without characteristic deterioration and destruction of IC.

Polarity of this voltage is determined by whether to apply voltage to - input terminal with reference to + input terminal, or apply voltage to + input terminal with reference to - input terminal.

Polarity is not of much concern, but what matters is how much voltage can be applied between input terminals.

However, it must be assumed that the potential of input terminal is above potential of V_{EE} terminal.

Rated differential input voltage is determined by withstand voltage of transistor connected to input terminal (such as NPN transistor and PNP transistor), etc.

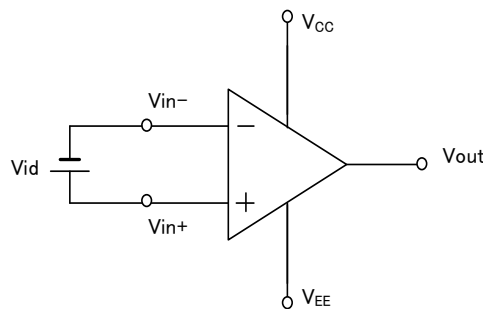


Fig. 2.2.1 Rated differential input voltage

2.3 Rated common mode input voltage

It refers to the maximum voltage that can be applied without characteristic deterioration or destruction of IC with + input terminal (non-inverting input terminal) and - input terminal (inverting input terminal) set at the same potential. Rated common mode input voltage is different from common mode input voltage range of electric characteristic item.

Rated common mode input voltage does not guarantee normal operation of IC. When expecting normal operation of IC, voltage within common mode input voltage range must be followed in the electric characteristic items.

Rated common mode input voltage is $V_{EE} - 0.3$ [V] and $V_{CC} + 0.3$ [V] in general, while the voltage up to power supply rating can be applied to some models. It is determined by protective circuit configuration of input terminal, withstand voltage of parasitic element and input transistor, etc.

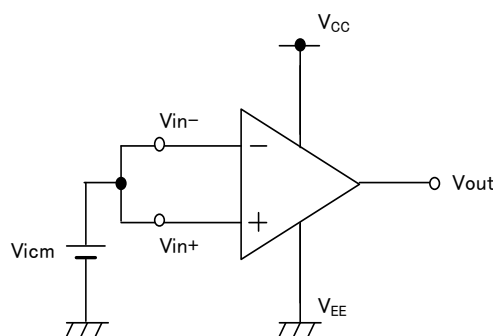


Fig. 2.3.1 Rated common mode input voltage

2.4 Maximum power dissipation and storage temperature range

Maximum power dissipation indicates an power which IC is capable of consuming at an ambient temperature $T_a = 25^\circ\text{C}$ (normal temperature). IC generates heat when it consumes power, and the temperature of chip becomes higher than ambient temperature. The temperature allowed in a chip is fixed, so that consumable power is limited.

Maximum power dissipation is determined by the temperature acceptable by IC chip in a package (junction temperature) and thermal resistance (heat dissipation) of package. The maximum value of junction temperature is normally equal to the maximum value of storage temperature range. Storage temperature range refers to a temperature range where IC can be stored without excessive deterioration of its characteristic. Heat generated by IC, when consuming power is dissipated from mold resin and lead frame of package. Parameter which shows this heat dissipation factor (hardness of heat to escape) is called thermal resistance, and is represented by $\theta_j = a[^\circ\text{C}/\text{W}]$. Temperature of IC inside the package can be estimated from this thermal resistance. Figure 2.4.1 shows a model of thermal resistance of package.

θ_{j-a} is represented by the sum of thermal resistance θ_{j-c} between chip cases (packages) and thermal resistance θ_{c-a} between a case (package) and outside. When thermal resistance θ_{j-a} , ambient temperature T_a , and power consumption P are known, chip temperature can be calculated by the equation below:

$$T_j = T_a + \theta_{j-a} \cdot P[\text{W}] \tag{2.4.1}$$

Figure 2.4.2 shows the thermal relaxing curve (degrading curve). This curve is a graph which shows how much power an IC can consume at some ambient temperature, and indicates power consumed by IC chip without exceeding allowable temperature. Let us consider chip temperature of BA4560RF (SOP8 plastic mold package) for an example. Storage temperature range of BA4560RF is between -55°C and 150°C , therefore the maximum allowable temperature of a chip is 150°C . Thermal resistance of SOP8 is $\theta_{j-a} \cong 181.8[^\circ\text{C}/\text{W}]$. When assuming that this IC consumes power 687 [mW] at $T_a = 25^\circ\text{C}$, junction temperature is calculated as follows:

$$T_j = 25[^\circ\text{C}] + 181.8[^\circ\text{C}/\text{W}] \cdot 0.687[\text{W}] \cong 150[^\circ\text{C}] \tag{2.4.2}$$

Therefore it is seen that the chip reaches its maximum allowable temperature, and no more electric can be consumed.

Chip junction—ambient thermal resistance
 $\theta_{j-a} = \theta_{j-c} + \theta_{c-a}[^\circ\text{C}/\text{W}]$
 where θ_{j-c} : junction—case(package) thermal resistance
 θ_{c-a} : case(package)—ambient thermal resistance

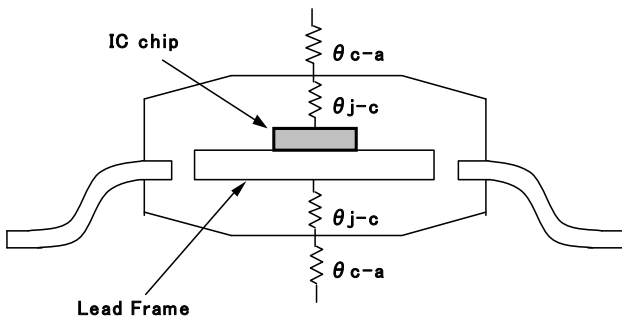


Fig.2.4.1 Thermal resistance of IC package

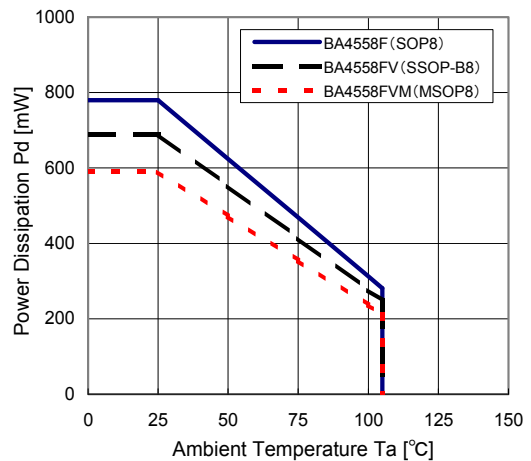


Fig.2.4.2 Power dissipation vs. Ambient temperature (Mounted 70mm x 70mm x 1.6mm FR4 glass epoxy board)

2.5 Electrostatic discharge tolerance

It represents a damage withstand capability against static electricity of IC, and is one of reliability test items. Example of damaging phenomenon when static electricity is applied to IC includes the phenomenon shown below:

Dielectric breakdown of film oxide

: Caused by high electric field applied to gate film oxide when the transistor has MOS structure.

Thermal breakdown of PN junction

: Excessive current flows in PN junction of device inside IC because of static electricity, which results in thermal breakdown of junction.

Melting of wiring

: When overcurrent flows in excess of allowable current of wiring, thermal breakdown occurs.

Test procedure used often for evaluating electrostatic discharge tolerance includes a human body model (HBM) and machine model. Human body model is a modeling of phenomenon in which electric charge on human body is discharged when it is in contact with a device, and machine model is a modeling of phenomenon in which electric charge on metallic equipment having greater capacity and smaller discharge resistance than human body is in contact with a device. Figure 2.5.1 shows a simple test circuit of human body model and machine model. Capacitance C_{ESD} is charged by high voltage, and discharged through resistance R_{ESD} for checking for breakdown. Capacitance / Resistance differ between human body model and machine model.

For human model : $C_{ESD} = 100[pF]$, $R_{ESD} = 1.5[k\Omega]$

For machine model : $C_{ESD} = 200[pF]$, $R_{ESD} = 0[\Omega]$

Common terminal in applying static electricity is V_{EE} terminal (GND terminal) and V_{CC} terminal in general. IC is generally provided with protective circuit against static electricity, and a measure is taken to prevent excessive current from flowing inside the circuit. When electrostatic surge occurs, in order to dissipate electric charge to common terminal without breakdown of internal circuit, current route with low impedance is reserved. Also, a resistor may be connected to a terminal in series in order to limit the amount of current. Example of protective circuit is shown in figure 2.5.2.

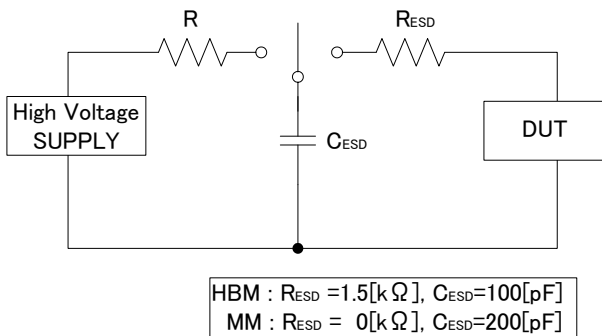


Fig. 2.5.1 HBM, MM simplified test circuit

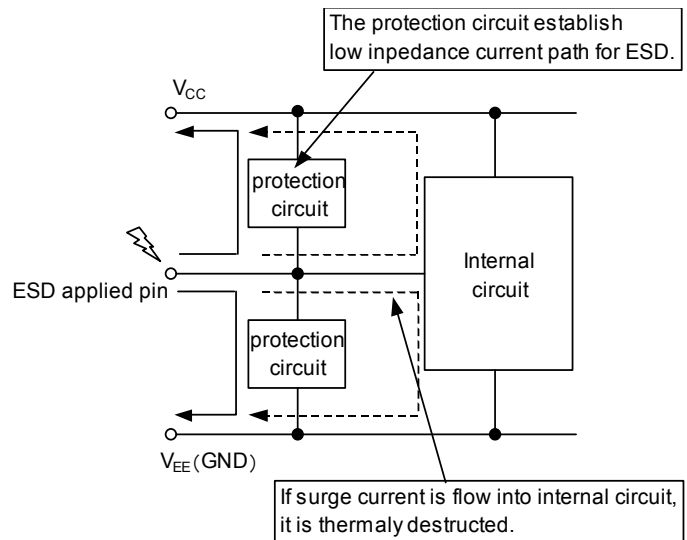


Fig. 2.5.2 Example of internal ESD protection

●3.Electrical characteristic of op-amp and comparator

Described here are the electric characteristic of op-amp/comparator and effect in actual use by use of an example.

3.1 Circuit current / quiescent current I_{cc} / I_q and power consumption

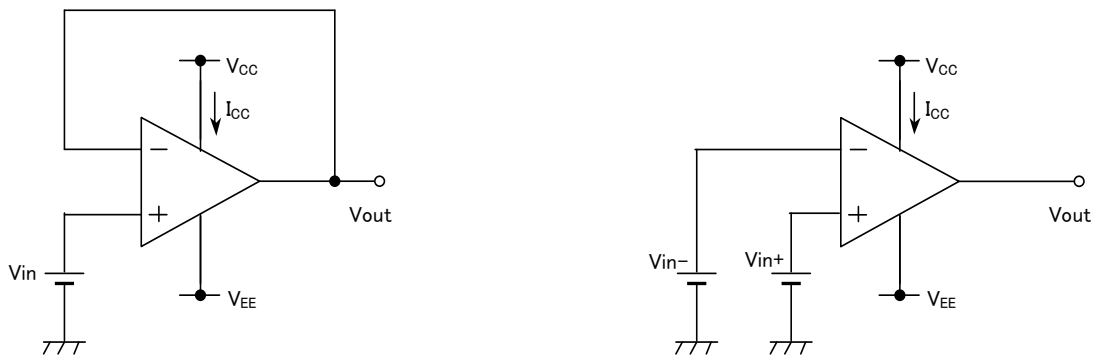
Standard value in specification indicates an current of op-amp/ comparator alone flowing under no-load, steady state as shown in figure 3.1.1. Measuring condition depends on a model. Actually, circuit current also changes because output current depends on load condition.

In calculating power consumption of op-amp/comparator, not only the circuit current but also the output current must be considered. How the power consumption is determined is indicated by use of figure 3.1.2 (a) and (b). Figure 3.1.2 (a) represents a state where the op-amp supplies output source current to the load. Here, the op-amp consumes the current of $I_{cc} + I_{out}$. Power consumption is calculated by multiplying the amperage by voltage. The current of I_{cc} and I_{out} flow along different routes, and the voltage applied to current route is different. Therefore, in calculating power consumption, it is necessary to divide into output current portion and circuit current portion excluding output current. Considering the description above, power consumption can be calculated by the equation below:

$$P = I_{cc} \cdot (V_{CC} - V_{EE}) + I_{out} \cdot (V_{CC} - V_{out}) \tag{3.1.1}$$

Figure 3.1.2 (b) shows the state where the op-amp supplies the output sink current to the load. Here, power consumption can be calculated by the following equation in the same concept as that in source current supply described above:

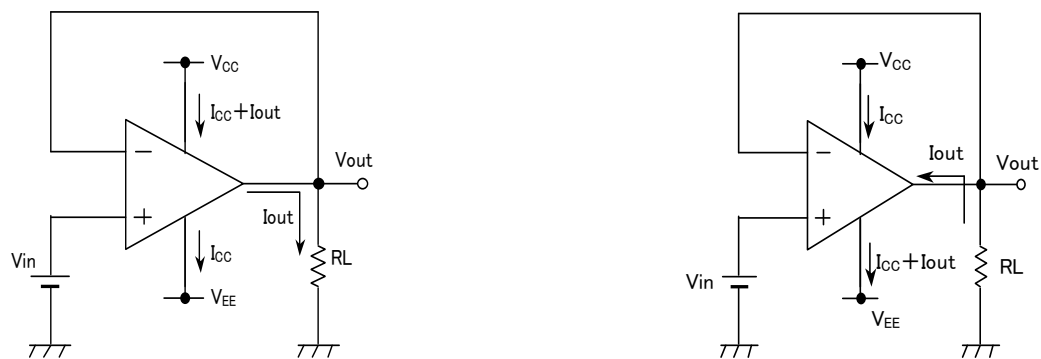
$$P = I_{cc} \cdot (V_{CC} - V_{EE}) + I_{out} \cdot (V_{out} - V_{EE}) \tag{3.1.2}$$



(a) Example of supply current test circuit for op-amp

(b) Example of supply current test circuit for comparator

Fig 3.1.1 Supply current of op-amp and comparator



(a) Current path of output source current

(b) Current path of output sink current

Fig. 3.1.2 Calculation of power dissipation

3.2 Input offset voltage V_{io}

It indicates the difference of potential between + input terminal and - input terminal. In other words, it is a voltage required for setting the output at 0[V]. Maximum input offset voltage is normally guaranteed under a given condition. The guaranteed value itself is indicated in absolute value. Input offset voltage is generated by voltage difference between the base and emitter of transistor connected to + input terminal and - input terminal (voltage difference between gate and source as for FET). It mainly results from the discrepancy of two transistor characteristics and asymmetry of circuit. This situation is shown in figure 3.2.1 (a), and modeling of op-amp including offset voltage is shown in (b). Input offset voltage actually depends on common mode input voltage, power supply voltage, ambient temperature, etc. Change by such use condition can be estimated by electric characteristic such as CMRR, PSRR, and temperature coefficient.

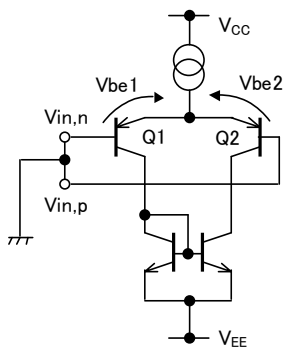
Effect of input offset voltage in actual use is considered, taking an example of circuit shown in figure 3.2.2. Figure 3.2.2 is a non-inverting amplifier with amplification factor $1 + R_2/R_1$. When we put the input offset voltage V_{io} , input voltage V_{in} , and output voltage V_{out} , the output voltage is given by the equation below:

$$V_{out} \cong (1 + (R_2/R_1)) \cdot (V_{in} + V_{io}) \tag{3.2.1}$$

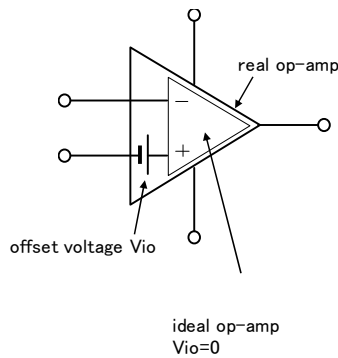
When we look at above equation, it can be seen that not only the input voltage but also the input offset voltage is amplified. When we put the input offset at 1[mV], it appears as an error of 100[mV] at the output from non-inversion amplifier with magnification factor 100[mV].

As an example of characteristics of input offset voltage, characteristic of input offset voltage - power supply voltage and characteristic of input offset voltage - temperature are shown in figure 3.2.3.

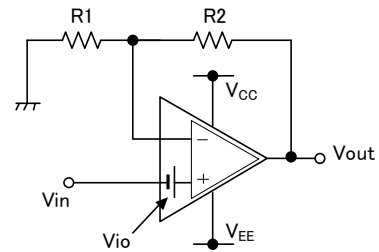
Basically, input offset voltage is occurred by base-emitter voltage difference of Q1 and Q2
 $(V_{in,n} + V_{be1} - V_{be2} - V_{in,p}) - V_{io} = 0$
 $V_{io} = V_{be1} - V_{be2}$



(a) example of op-amp input stage



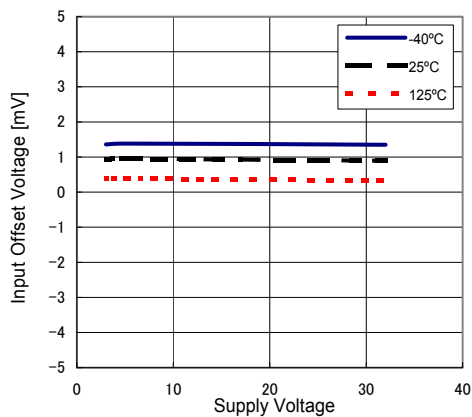
(b) input offset voltage model



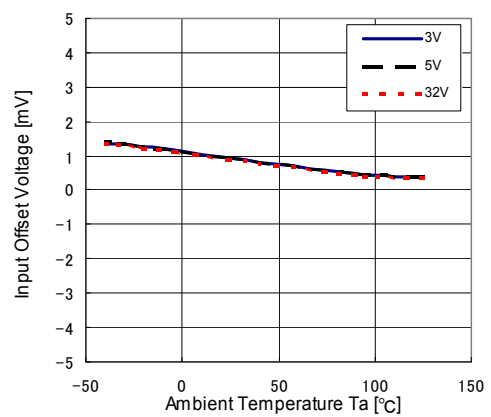
the circuit equations are following,
 $V_{out} = a \cdot (V_{in} + V_{io} - V_{in,n})$
 $(0 - V_{in,n}) / R_1 = (V_{in,n} - V_{out}) / R_2$
 $\therefore V_{out} \cong (1 + (R_2/R_1)) \cdot (V_{in} + V_{io})$
 Input offset voltage is increased by voltage gain

Fig. 3.2.2 influence of input offset voltage

Fig. 3.2.1 The model of input offset voltage



(a) BA2904F input offset voltage—supply voltage



(b) BA2904F input offset voltage—ambient temperature

Fig. 3.2.3 example of input offset voltage characteristic

3.3 Input bias current/Input offset current Ib/Iio

Input bias current is a current which flows into input terminal or flows out of input terminal. Direction of current depends on the type of transistor connected to input terminal. In the case of bipolar structure in general, direction flowing into input terminal is applied to NPN transistor, and direction flowing out of input terminal is applied to PNP transistor. Input offset current is the difference of input bias current respectively of + input terminal and - input terminal. When we put the bias current of + input terminal and - input terminal $I_{b,p}$ and $I_{b,n}$, respectively. The input bias current I_b and input offset current I_{io} are defined by the equation below:

$$I_b = (I_{b,p} + I_{b,n}) / 2 \tag{3.3.1}$$

$$I_{io} = I_{b,p} - I_{b,n} \tag{3.3.2}$$

Input terminal of op-amp/comparator is connected to the base of transistor for bipolar structure, and to the gate of transistor for FET structure in order to provide high input resistance. For this reason, the input bias current is either the base current or gate current of transistor, and is in general on the order of nA - μ A for bipolar structure, and on the order of fA - pA for FET structure.

Take an example of figure 3.3.2 in considering the effect by input bias current and input offset current in actual use. Figure 3.3.2 shows a non-inverting amplifier. When we put the input voltage at V_{in} and output voltage at V_{out} , the output voltage is calculated by the equation below:

$$V_{out} = -(R_2/R_1) \cdot V_{in} - (1 + R_2/R_1) \cdot ((R_1/R_2) \cdot I_{b,n} - R_3 \cdot I_{b,p}) \tag{3.3.3}$$

$$= -(R_2/R_1) \cdot V_{in} - (1 + R_2/R_1) \cdot ((R_1/R_2 - R_3) \cdot I_b - (R_1/R_2 + R_3) \cdot I_{io}/2) \tag{3.3.4}$$

When we choose R_3 so that $R_3 = R_1/R_2$, the term of error by input bias current can be eliminated. Here, the output voltage V_{out} is given by the equation below:

$$V_{out} = -(R_2/R_1) \cdot V_{in} + (1 + R_2/R_1) \cdot ((R_1/R_2) \cdot I_{io}) \tag{3.3.5}$$

Figure 3.3.3 shows an example of temperature characteristics of input bias current and input offset current.

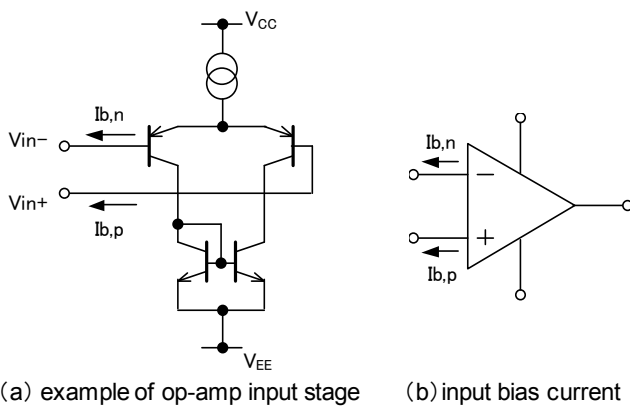
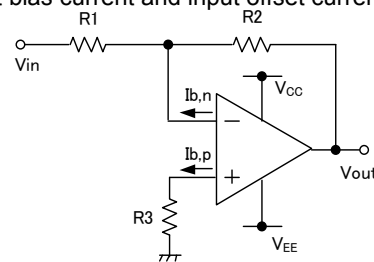
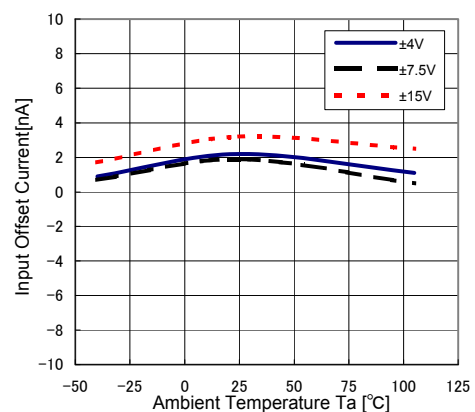
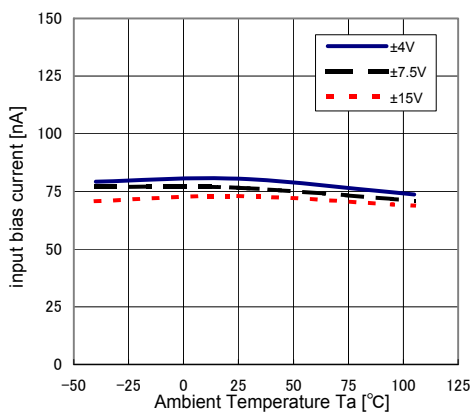


Fig. 3.3.1 input bias current



The constructed feedback circuit behaves linear circuit. Therefore superposition criterion is consisting. Output error voltage occurred by input bias current and input offset current is following.
 $V_{in,p} = V_{in,n} = R_3 \cdot I_{b,p}$
 $I_{b,n} = V_{in,p} / R_1 + (V_{in,p} - E_{out}) / R_2$
 $\therefore E_{out} = (1 + R_2/R_1) \cdot ((R_1/R_2) \cdot I_{b,n} - R_3 \cdot I_{b,p})$
 $= (1 + R_2/R_1) \cdot ((R_1/R_2 - R_3) \cdot I_b - (R_1/R_2 + R_3) \cdot I_{io}/2)$

Fig 3.3.2 influence of input bias current and input offset current



(a) BA4560RF input bias current - ambient temperature (b) BA4560RF input offset current - ambient temperature

Fig. 3.3.3 input bias current and input offset current - temperature characteristic

3.4 Common mode input voltage range Vicm / CMR

It indicates an input voltage range where the op-amp/comparator operates normally. If any voltage out of common mode input voltage range is applied, desired output voltage cannot be obtained. Common mode input voltage range is determined mainly by configuration of input step circuit (configuration of differential amplifier circuit). Figure 3.4.1 shows the input step circuit configuration of op-amp of BA4558R and BA2904. IC op-amp must operate normally within common mode input voltage range, therefore all transistors on input step must operate in linear area. In the circuit shown in figure 3.4.1, the upper limit of common mode input voltage is an input voltage where Q0 is not saturated, and the lower limit of common mode input voltage is an input voltage where Q1 and Q2 are not saturated. When we put the voltage between base and emitter of each transistor at Vbe, and the voltage between collector and emitter at Vsat where the transistor begins to be saturated, the common mode input voltage range of op-amp of BA4558R and BA2904 is as shown below:

$$\text{Common mode input voltage range of op-amp of BA4558R} \\ -V_{be2} + V_{be5} + V_{be6} + V_{sat2} + V_{EE} < V_{icm} < V_{CC} - V_{be2} - V_{sat0} \tag{3.4.1}$$

$$\text{Common mode input voltage range of op-amp of BA2904} \\ -V_{be1}' - V_{be1} + V_{be3} + V_{sat1} + V_{EE} < V_{icm} < V_{CC} - V_{be1}' - V_{be1} - V_{sat0} \tag{3.4.2}$$

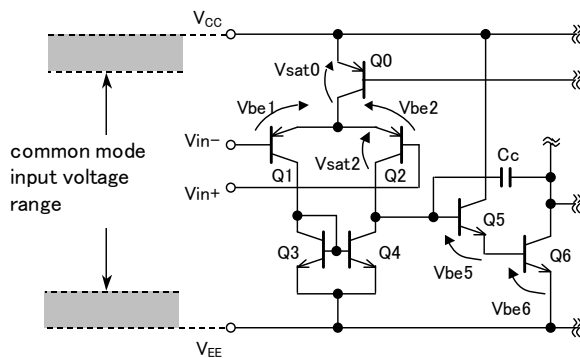
When it is assumed that all Vbe equal to Vsat,

$$\text{Common mode input voltage range of op-amp of BA4558R} \\ V_{EE} + (V_{be} + V_{sat}) < V_{icm} < V_{CC} - (V_{be} + V_{sat}) \tag{3.4.3}$$

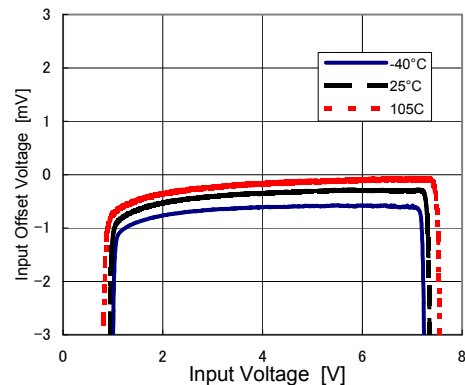
$$\text{Common mode input voltage range of op-amp of BA2904} \\ V_{EE} + (-V_{be} + V_{sat}) < V_{icm} < V_{CC} - (2 \cdot V_{be} - V_{sat}) \tag{3.4.4}$$

The lower limit of common mode input voltage range of op-amp of BA4558 is determined by the common mode input voltage where Q2 is saturated because the collector potential of Q2 is higher than that of Q1, and Q1 has an input voltage higher than Q2 where they come into saturation region. Op-amp of BA2904 uses a level shift circuit (Q1' and Q2') so that it can apply GND potential for input voltage. The circuit is configured so that the collector potential of Q1 and Q2 is almost equal.

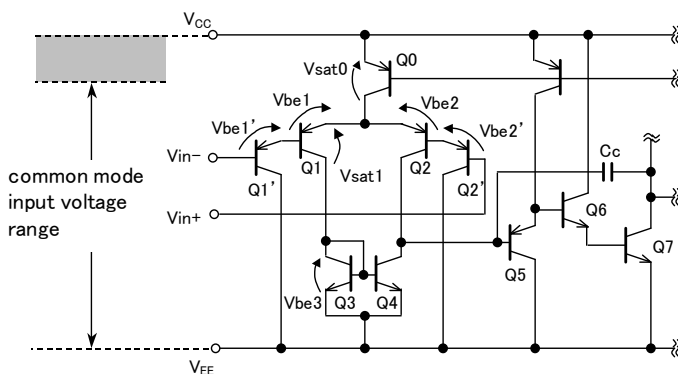
Therefore, Q1 and Q2 are saturated at an almost equal input voltage. When we look at the formula above, the lower limit of common mode input voltage range of op-amp of BA2904 is normally higher for Vbe than for Vsat, and it can be seen that VEE potential (GND potential) is included. Op-amp which thus allows input of VEE potential (GND potential) is called a single power supply op-amp. It is impossible to input GND (VEE) potential for input voltage by use of op-amp such as BA4558R, which is designed for both power sources beforehand, but it can be used sufficiently by single power source when appropriate input voltage is set.



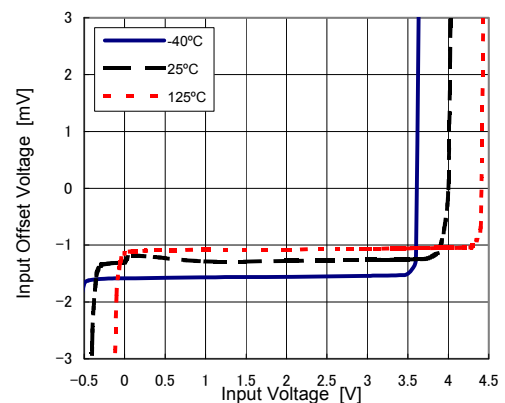
(a) BA4558RF input stage simplified schematic



(b) BA4558RF input offset voltage - input voltage



(c) BA2904F input stage simplified schematic



(d) BA2904F input offset voltage - input voltage

Fig.3.4.1 BA4558RF and BA2904F input common mode voltage range

3.5 Maximum output voltage (output voltage range) Vom / Voh, Voi

It refers to a voltage range which can be output by op-amp. Voltage is divided into high level output voltage and low level output voltage. Output voltage range is limited by output circuit configuration, power supply voltage, and load condition (output current). Take an example of op-amp of BA4558R and BA2904 shown in figure 3.5.1 to see how the maximum output voltage is limited by output circuit configuration. Figure 3.5.1 (a) shows an output equivalent circuit of BA4558R. High level output voltage of this circuit is limited by saturation voltage of Q1, voltage between base and emitter of Q2 and output protection resistor R1. Low level output voltage is limited by saturation voltage of Q4, voltage between base and emitter of Q3, and output protection resistor R2. The smaller the load resistance is and the greater the output current is, the greater is the voltage fall because of saturation voltage of each transistor, voltage between the base and emitter, and protection resistance, which makes the output voltage range smaller. Output voltage of BA4558R is determined by the equation below:

$$V_{oh} = V_{CC} - (V_{ce1} + V_{be2} + R1 \cdot I_{source}) \tag{3.5.1}$$

$$V_{ol} = V_{EE} + (V_{ce4} + V_{be3} + R2 \cdot I_{sink}) \tag{3.5.2}$$

I_{source} represents the output source current, and I_{sink} the output sink current. Figure 3.5.1 (b) shows the output voltage - load resistance characteristics of BA4558RF.

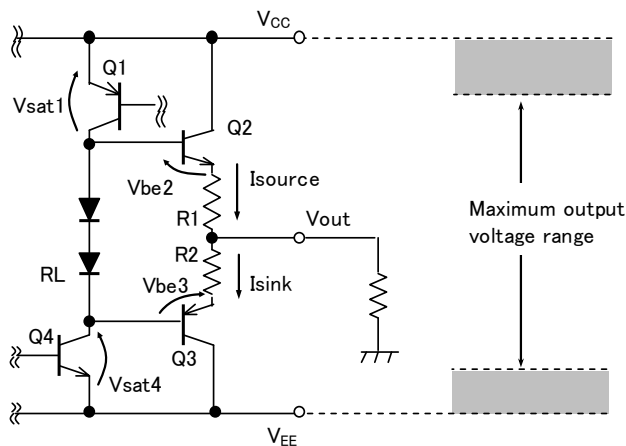
Figure 3.5.1 (c) shows an output equivalent circuit of op-amp of BA2904. High level output voltage is determined by the voltage between collector and emitter of Q1, voltage between base and emitter of Q2, and voltage between base and emitter of Q3, and voltage fall by R1. Low level output voltage depends on the amount of sink current. Fixed current source of 50μA is connected to the output terminal of op-amp of BA2904, and the voltage close to GND level can be output until sink current is several ten μA. When sink current exceeds this amperage, Q4 starts to be conductive, so that the low level output voltage is limited by the voltage between collector and emitter of Q5, and voltage between base and emitter of Q4. Output voltage of BA2904 is determined by the equation below:

$$V_{oh} = V_{CC} - (V_{sat1} + V_{be2} + V_{be3} + R1 \cdot I_{source}) \tag{3.5.3}$$

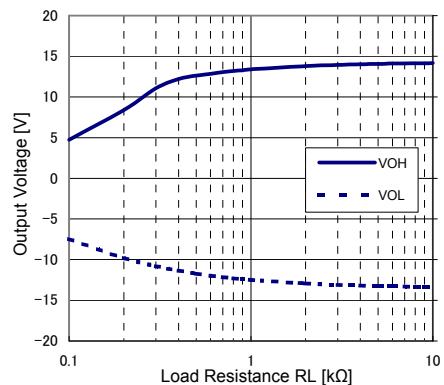
$$V_{ol} = V_{ce6} \quad (I_{sink} < \text{several ten } \mu A) \tag{3.5.4}$$

$$= V_{ce5} + V_{be4} \quad (I_{sink} > \text{several ten } \mu A) \tag{3.5.5}$$

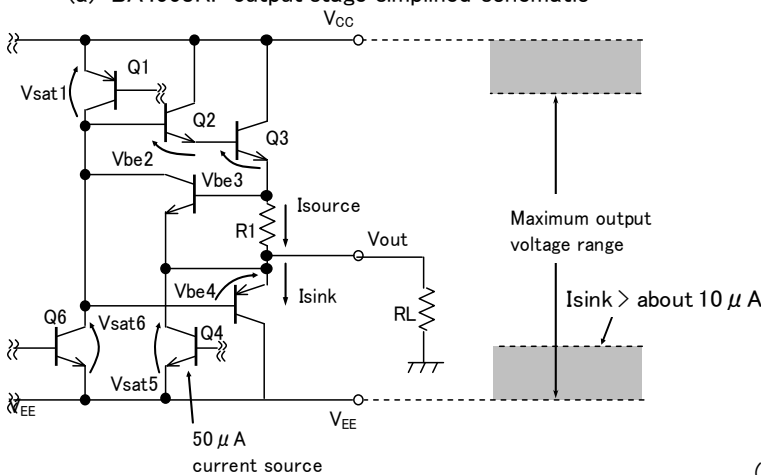
Figure 3.5.1 (d) shows the characteristic of output voltage - output current of BA2904F.



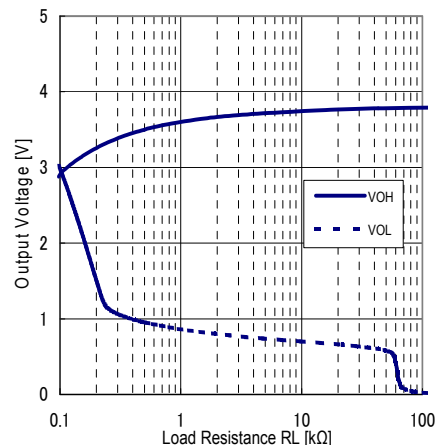
(a) BA4558RF output stage simplified schematic



(b) BA4558RF output voltage vs load resistance (V_{CC}=15[V], V_{EE}=-15[V], T_a=25[°C])



(c) BA2904F output stage simplified schematic



(d) BA2904F output voltage vs load resistance (V_{CC}=5[V], V_{EE}=0[V], T_a=25[°C])

Fig. 3.5.1 BA4558RF, BA2904F output voltage range

3.6 Common Mode Rejection Ratio (CMRR)

It refers to the ratio of fluctuation of input offset voltage when input voltage is changed. Standard of specification refers to the ratio of fluctuation of input offset current when DC input voltage is changed.

$$CMRR = \Delta V_{icm} / \Delta V_{io} \tag{3.6.1}$$

Definition of CMRR is the ratio between amplification factor A_d of amplifier with reference to input voltage difference and amplification factor A_c with reference to common mode input voltage, $CMRR = A_d/A_c$, which means the same thing as the equation (3.6.1). It is ideal for an op-amp to increase the potential difference between + input terminal and - input terminal by the amplification factor provided for the amplifier, while DC operation point inside the circuit is changed by changing common mode input voltage on actual op-amp, therefore the output voltage fluctuate slightly. When we put the amplification factor with reference to the input differential voltage of op-amp at A_d , the amplification factor with reference to the common mode input voltage at A_c , the potential of + input terminal at $V_{in,p}$, and the potential of - input terminal at $V_{in,n}$, then the output voltage from op-amp is represented by the equation below:

$$V_{out} = A_d \cdot (V_{in,p} - V_{in,n}) + A_c \cdot V_{ic} \tag{3.6.2}$$

$$= A_d \cdot ((V_{in,p} - V_{in,n}) + (A_c/A_d) \cdot V_{ic}) \tag{3.6.3}$$

Where, V_{ic} is the common mode input voltage, and equals to $(V_{in,p} + V_{in,n})/2$. The term $(A_c/A_d) V_{ic}$ in the equation above represents an error term by common mode input voltage, and can be considered to be an input offset voltage.

$$V_{io,ic} = (A_c/A_d) \cdot V_{ic} \tag{3.6.4}$$

Fluctuation of input offset voltage with reference to the change of common mode input voltage is calculated as follows by this relation:

$$\Delta V_{ic} / \Delta V_{io,ic} = A_d/A_c = CMRR \tag{3.6.5}$$

We understand that this is equal to the ratio between the amplification factor A_d of input voltage difference and the amplification factor of common mode input voltage mentioned above.

Let us consider the effect by the change of common mode input voltage in actual use taking an example of non-inversion amplifier in figure 3.6.1. When we put the input offset voltage by $V_{ic} = 0[V]$ on op-amp at $V_{io,0}$, then the input offset voltage $V_{io,10}$ by $V_{ic} = 10[V]$ is calculated as follows:

$$V_{io,10} = V_{io,0} + 10[V]/CMRR \tag{3.6.6}$$

When $V_{io,0} = 1[mV]$ and $CMRR = 80[dB]$, the input offset voltage $V_{io,1}$ by $V_{ic} = 10[V]$ is $2[mV]$. Therefore, it appears as an error of $200[mV]$ on the output voltage if non-inverting amplifier with magnification factor 100 is used. Also, CMRR depends on signal frequency, and attenuates as the frequency becomes the higher.

Figure 3.6.2 shows an example of input offset voltage - common mode input voltage characteristics and common mode rejection ratio frequency characteristics.

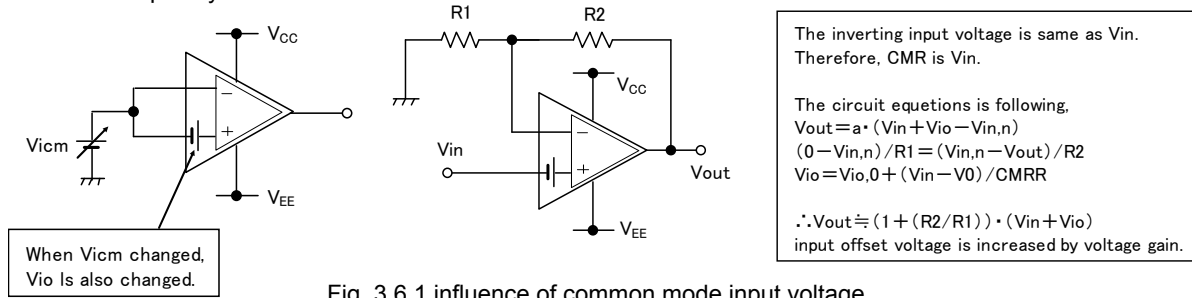


Fig. 3.6.1 influence of common mode input voltage

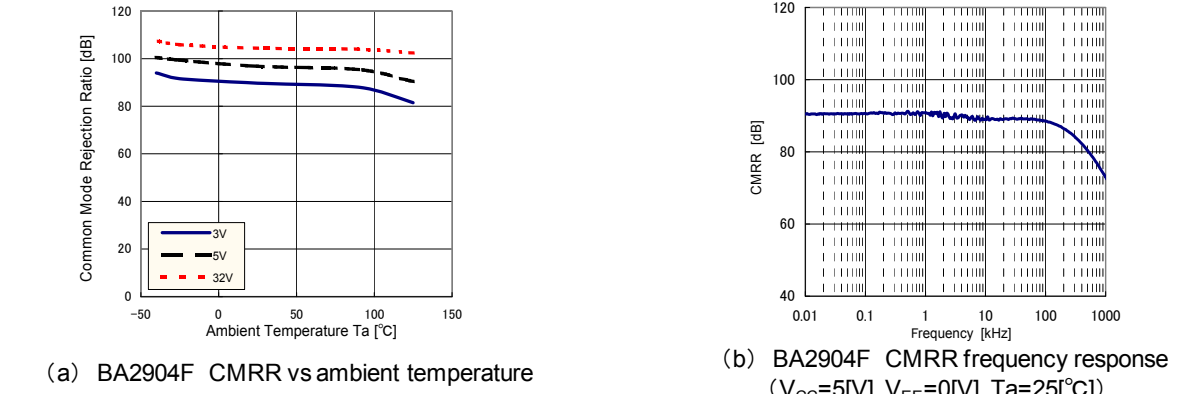


Fig. 3.6.2 example of CMRR characteristics

3.7 Power Supply Rejection Ratio (PSRR)

It refers to the ratio of fluctuation of input offset voltage when power supply voltage is changed. Standard of specification indicates the ratio of fluctuation of input offset current when DC power supply voltage is changed.

$$PSRR = \Delta(V_{CC} - V_{EE}) / \Delta V_{io} \tag{3.7.1}$$

Definition of PSRR is the ratio between amplification factor A_d of amplifier with reference to input voltage difference and amplification factor A_p with reference to power supply voltage, $PSRR = A_d/A_p$, which means the same thing as the equation (3.7.1). It is ideal for an op-amp to increase the potential difference between + input terminal and - input terminal by the amplification factor provided for the amplifier, while DC operation point inside the circuit is changed by changing power supply voltage on actual op-amp, therefore the output voltage fluctuate slightly. When we put the amplification factor with reference to the input differential voltage of op-amp at A_d , the amplification factor with reference to the power supply voltage at A_p , the potential of + input terminal at V_{in+} , and the potential of - input terminal at V_{in-} , then the output voltage from op-amp is represented by the equation below:

$$V_{out} = A_d \cdot (V_{in+} - V_{in-}) + A_p \cdot V_{CC} \tag{3.7.2}$$

$$= A_d \cdot ((V_{in+} - V_{in-}) + (A_p/A_d) \cdot V_{CC}) \tag{3.7.3}$$

The term $(A_p/A_d) V_{CC}$ in the equation above represents an error term by power supply voltage, and can be considered to be an input offset voltage.

$$V_{io,ps} = (A_p/A_d) \cdot V_{CC} \tag{3.7.4}$$

Fluctuation of input offset voltage with reference to the change of power supply voltage is calculated as follows by this relation:

$$\Delta V_{CC} / \Delta V_{io,ps} = A_p/A_d = PSRR \tag{3.7.5}$$

We understand that PSRR is equal to the ratio between the amplification factor A_d of input voltage difference and the amplification factor of power supply voltage A_p mentioned above.

Let us consider the effect by the change of power supply voltage in actual use taking an example of non-inversion amplifier in figure 3.7.2. When we put the input offset voltage by $V_{CC} = 10[V]$ on op-amp at $V_{io,10}$, then the input offset voltage $V_{io,20}$ by $V_{CC} = 20[V]$ is calculated as follows:

$$V_{io,20} = V_{io,10} + 10[V]/PSRR \tag{3.7.6}$$

When $V_{io,10} = 1[mV]$ and $PSRR = 80[dB]$, the input offset voltage $V_{io,20}$ by $V_{CC} = 20[V]$ is $2[mV]$. Therefore, it appears as an error of $200[mV]$ on the output voltage if non-inverting amplifier with magnification factor 100 is used. In this connection, PSRR attenuates when the frequency increases. Therefore the existence of ripple with high frequency on power supply line leads to great fluctuation of output voltage. This effect can be suppressed by connecting a bypass capacitor near the op-amp. Figure 3.7.2 shows an example of input offset voltage - power supply voltage characteristics and power supply rejection ratio characteristics.

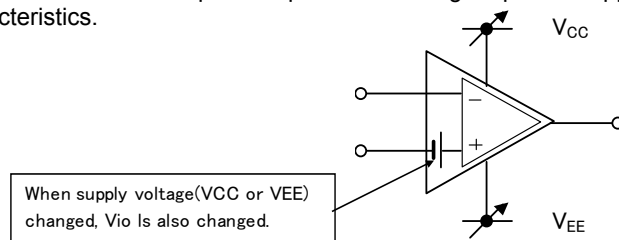


Fig. 3.7.1 Supply voltage dependence of input offset voltage

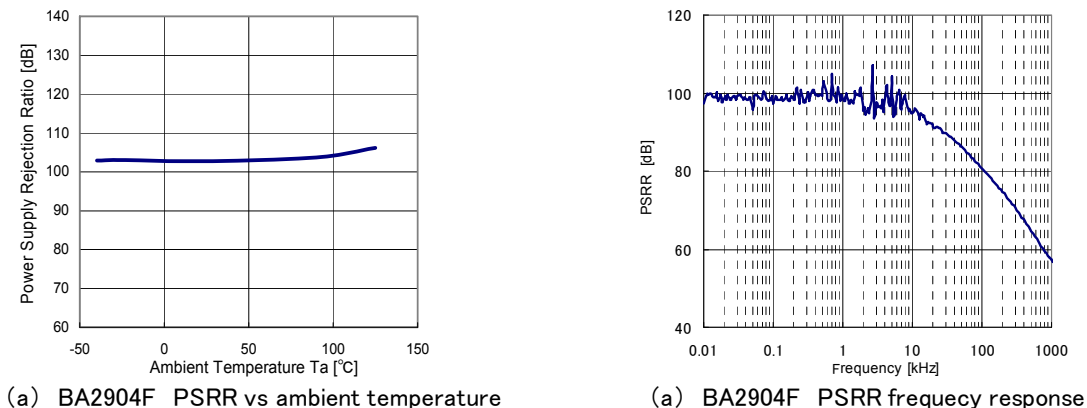


Fig. 3.7.2 example of PSRR characteristics

3.8 Large signal voltage gain (large amplitude voltage gain, open loop voltage gain) A_v

It refers to an amplification factor with reference to differential voltage between + input terminal and - input terminal of op-amp/comparator. The standard shows voltage gain with reference to DC voltage. High gain is preferable in general because it is desired to make gain error as small as possible generated when feedback circuit is configured. When we put the output voltage at V_{out} and input potential difference at $V_{in,d}$, then the voltage gain A_v is given by the equation below:

$$A_v = V_{out} / V_{in,d} \tag{3.8.1}$$

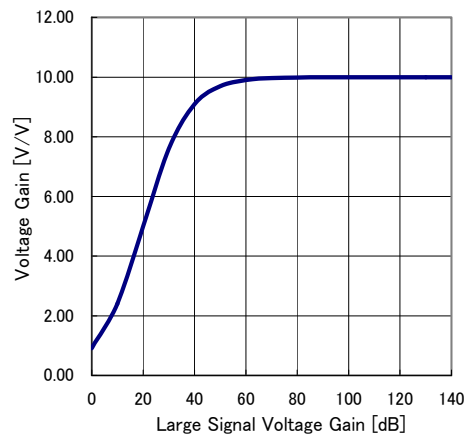
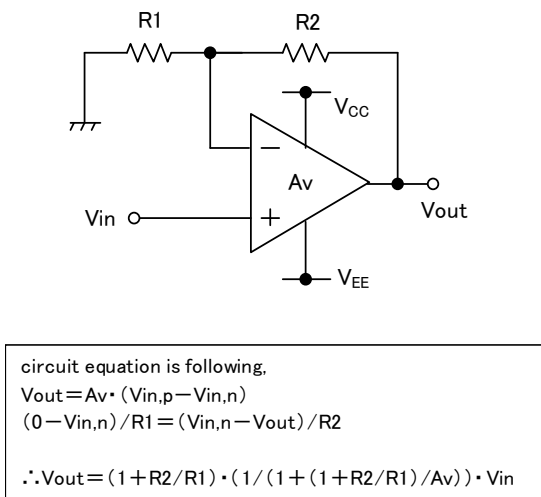
Take an example of circuit in figure 3.8.1 to consider the gain error. This figure shows a non-inverting amplifying circuit, and output voltage V_{out} is calculated as follows:

$$V_{out} = (1 + R_2/R_1) \cdot (1 / (1 + (1 + R_2/R_1) / A_v)) \cdot V_{in} \tag{3.8.2}$$

When we put $R_1 = 1 [k\Omega]$, $R_2 = 10[k\Omega]$, and $A_v = 80dB$, this value is calculated as follows:

$$V_{out} = 10.988 \cdot V_{in} \tag{3.8.3}$$

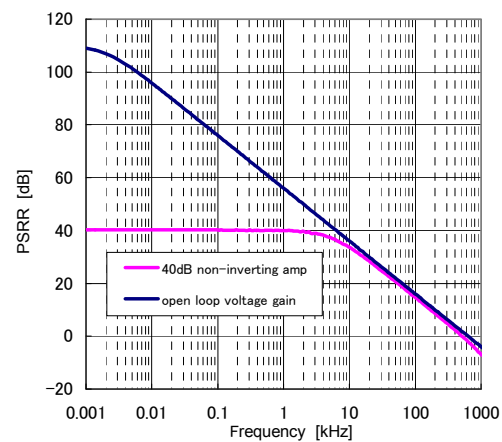
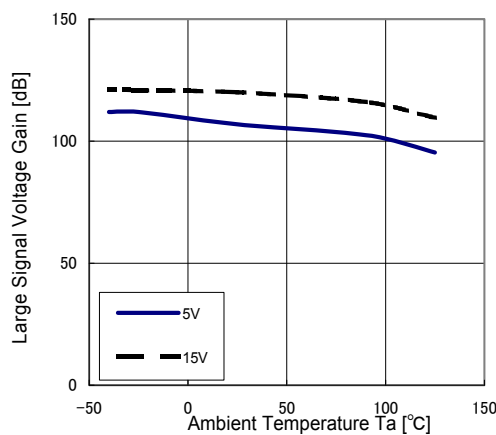
It is smaller than the ideal amplification factor 11. Voltage gain depends on frequency, and attenuates as the input signal frequency becomes the higher. Therefore, the greater the frequency is, the greater is the gain error. Figure 3.8.2 shows an example of voltage gain temperature characteristics and voltage gain frequency characteristics.



(a) inverting amplifier

(b) dependence of open loop voltage gain for 20dB inverting amplifier

Fig. 3.8.1 influence of open loop voltage gain



(a) BA2904F large signal voltage gain vs ambient temperature ($R_L = 2 [k\Omega]$)

(b) BA2904F large signal voltage gain frequency response ($V_{CC} = 5[V]$, $R_L = 2[k\Omega]$)

Fig. 3.8.2 example of large signal voltage gain characteristics

3.9 Slew Rate (SR)

It is a parameter which refers to the operation speed of op-amp. It refers to at what rate of time the output voltage rises or falls when square wave pulse is applied to the input. Figure 3.9.1 shows the waveform of input/output voltage. Slew rate makes it possible to estimate what degree of frequency signal can be applied. Figure 3.9.2 shows the waveform of output voltage when the sine wave is applied to op amp. When we put the output voltage at $V_{out}(t)$, amplitude at A , and signal frequency at f , then $V_{out}(t)$ can be calculated by the equation below:

$$V_{out}(t) = A \cdot \sin(2\pi \cdot f \cdot t) \tag{3.9.1}$$

When it is differentiated by t ,

$$\frac{dV_{out}(t)}{dt} = 2\pi \cdot f \cdot A \cdot \sin(2\pi \cdot f \cdot t) \tag{3.9.2}$$

The time t when this slope becomes the maximum is when the sine wave reaches the intermediate potential, which is shown by the equation below:

$$\frac{dV_{out}(t)}{dt} |_{max} = 2\pi \cdot f \cdot A \tag{3.9.3}$$

In order that a signal is output without restriction by slew rate, the maximum inclination in the equation above must be smaller than slew rate.

$$SR > 2\pi \cdot f \cdot A \tag{3.9.4}$$

For example, when you want to make the op-amp with slew rate 1.0 [V/μs] output a sine wave with amplitude 5[Vp-p], acceptable signal frequency is limited to the frequency which satisfies the equation below:

$$f < SR / (2 \cdot \pi \cdot A) = 1.0[V/\mu s] / 2 \cdot \pi \cdot 5[V_{p-p}] = 31.83[kHz] \tag{3.9.5}$$

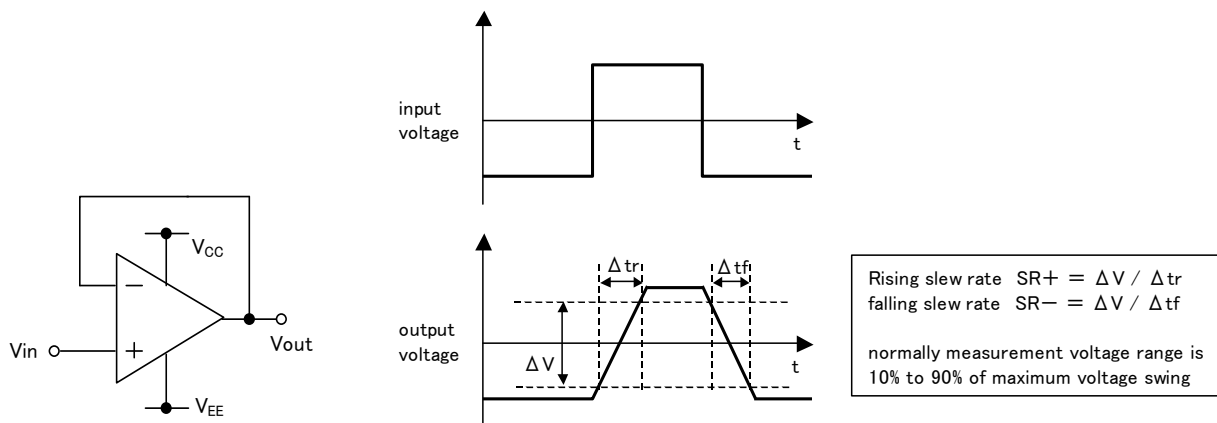


Fig. 3.9.1 slew rate

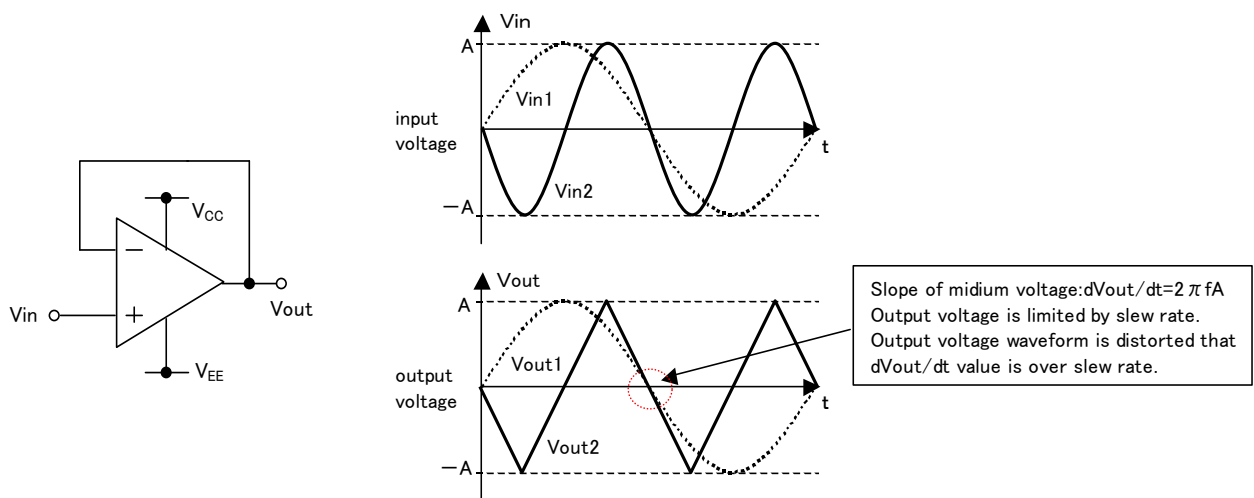


Fig. 3.9.2 input and output waveform applied sine wave

3.10 Response time t_{re} / t_{pHL} / t_{pLH}

It is a parameter which shows in what time period a pulse is output when square wave pulse is applied to a comparator. It is normally measured by the time period when a voltage reaches 50% of output voltage amplitude, starting from reference voltage. Figure 3.10.1 shows the input/output waveform of comparator and op-amp. Rising time and falling time of output waveform from op-amp containing phase compensation capacitance are limited by slew rate. Slew rate is determined by the time to charge/discharge the phase compensation capacitance. Comparator has no phase compensation capacitance, and responses in rising time and falling time is earlier than op-amp. In evaluating the response time of comparator, the potential difference between reference voltage and signal level, called overdrive, is changed in evaluation. Here, response time is measured by the time period from reference voltage up to 50% of output amplitude. It is also possible that the response time is measured by applying an input signal of TTL level (3.5 [Vp-p]).

Comparator of BA10393 and BA10339 etc, is an output circuit of open collector type. In this output type, rising time becomes shorter because the output NPN transistor drives the load directly. Rising time is limited by external pull-up resistor, load capacitance (contain parasitic capacitance).

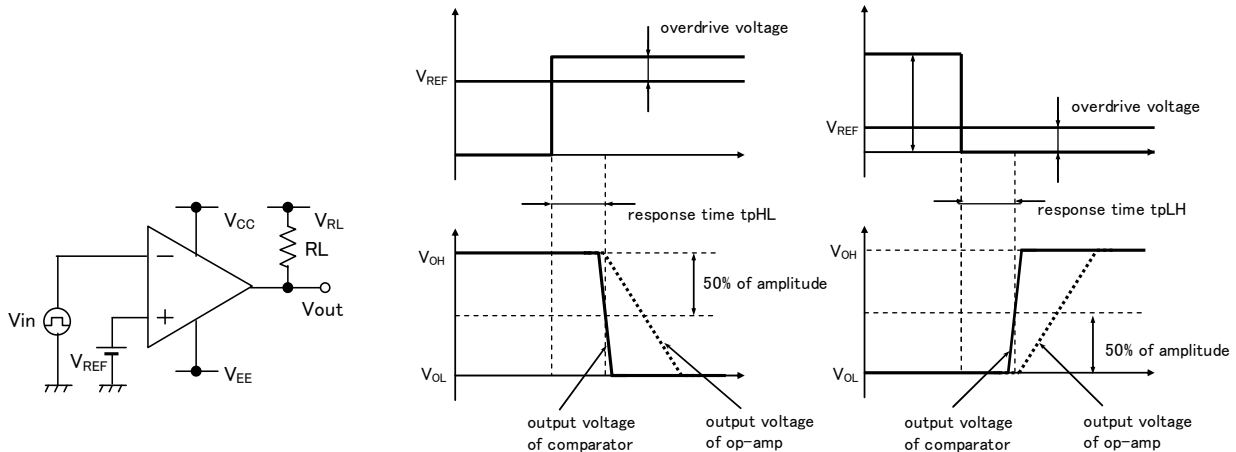
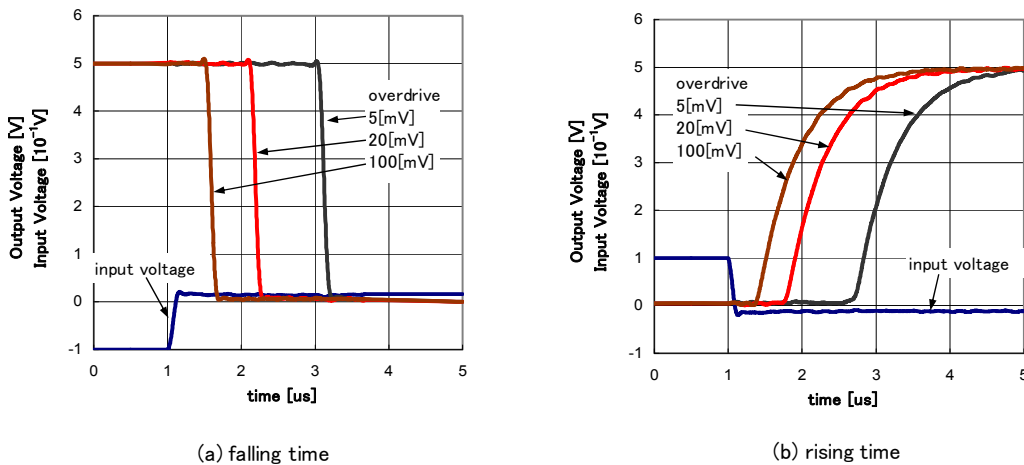
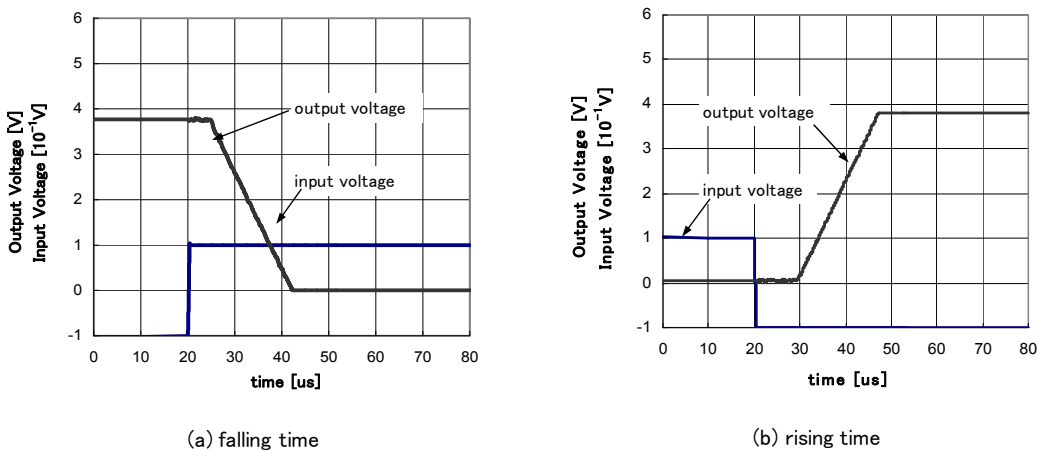


Fig. 3.10.1 response time of op-amp and comparator



(a) falling time (b) rising time
Fig. 3.10.2 BA2903F response time (pull-up resistor 5.1[kΩ], Vcc=5V)



(a) falling time (b) rising time
Fig. 3.10.3 BA2904F response time (load resistance 10[kΩ], Vcc=5V, 100mV overdrive)

3.11 Open loop voltage gain frequency characteristics and unity gain frequency/gain bandwidth product

Figure 3.11.1 shows the open loop voltage gain frequency characteristics. Op-amp can be considered to be an integrator, and has a high voltage gain by DC, while reduces the gain as the signal frequency becomes the higher. Important parameters of frequency characteristics are phase margin, gain margin and unity gain frequency. Phase margin ϕ_m is a parameter which shows how much margin a phase has with reference to 180 degrees when the gain is unity. Gain margin GM shows how small the gain is with reference to unity when the phase is delayed 180 degrees. Unity gain frequency f_t is a frequency when the gain is 1. When we put the voltage gain frequency characteristics of op-amp at $a(f)$, phase margin ϕ_m and gain margin GM are represented by the equation below:

$$\phi_m = 180^\circ - |\angle a(f)| \tag{3.11.1}$$

$$GM = 20 \log (1 / |a(f_{-180^\circ})|) \tag{3.11.2}$$

Terms for estimating unity gain frequency include a parameter called gain bandwidth product (GBW). Gain bandwidth product is a parameter for estimating f_t assuming that the op-amp is a simple first order integrator. With use of this assumption, the voltage gain frequency characteristics of op-amp are represented by the equation below:

$$a(f) = a_0 / (1 + j(f / f_{-3dB})) \tag{3.11.3}$$

" a_0 " is a voltage gain with reference to DC voltage. (Same as the large signal voltage gain A_v in section 3.9)

The magnitude of $a(f)$ is given by the equation below:

$$|a(f)| = a_0 / (1 + (f / f_{-3dB})^2)^{1/2} \tag{3.11.4}$$

In the equation above, the frequency which satisfies $f \gg f_{-3dB}$ and the magnitude of voltage gain when $f = f_t$ are shown respectively by the equation below:

$$f \gg f_{-3dB} \quad a(f) \doteq a_0 / (f / f_{-3dB}) \quad \Rightarrow \quad |a(f)| \cdot f = a_0 \cdot f_{-3dB} \tag{3.11.5}$$

$$f = f_t \quad |a(f_t)| \doteq a_0 / (f_t / f_{-3dB}) = 1 \quad \Rightarrow \quad f_t = a_0 \cdot f_{-3dB} \tag{3.11.6}$$

The relation below is established by the two equations above.

$$|a(f)| \cdot f = f_t \tag{3.11.7}$$

This relation means that the product of gain and frequency can always be approximate to f_t in a frequency range which satisfies $f \gg f_{-3dB}$.

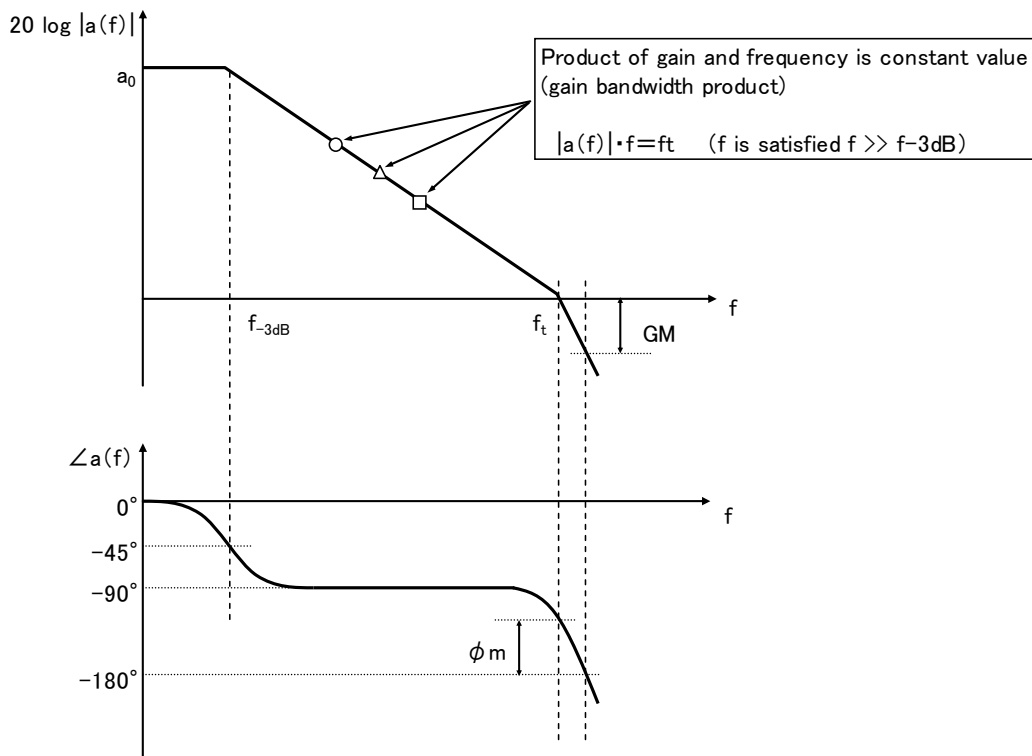


Fig. 3.11.1 open loop voltage gain (large signal voltage gain) frequency response

3.12 Model of negative feedback system and oscillation condition

Op-amp is seldom used alone, but is used in configuration of negative feedback circuit. One of things that should be noted in configuration of feedback circuit is the stability. Here, the stability of feedback circuit is described in the main.

3.12.1 Model of negative feedback system and oscillation condition

Model of negative feedback system is shown in figure 3.12.1. Transfer function between input and output is calculated by use of this model. "a(f)" is the amplification factor of amplifier, and β(f) is a feedback factor determined by feedback circuit. Transfer function A(f) between input and output is calculated by the equation below:

$$A(f) = V_{out}/V_{in} = a(f) / (1 + \beta(f) \cdot a(f)) \tag{3.12.1}$$

$$= a(f) \cdot (1 + T(f))^{-1} \tag{3.12.2}$$

$$= (1 / \beta(f)) \cdot (1 + 1/T(f))^{-1} \tag{3.12.3}$$

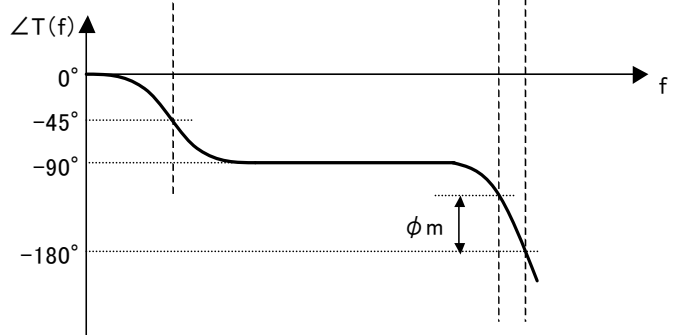
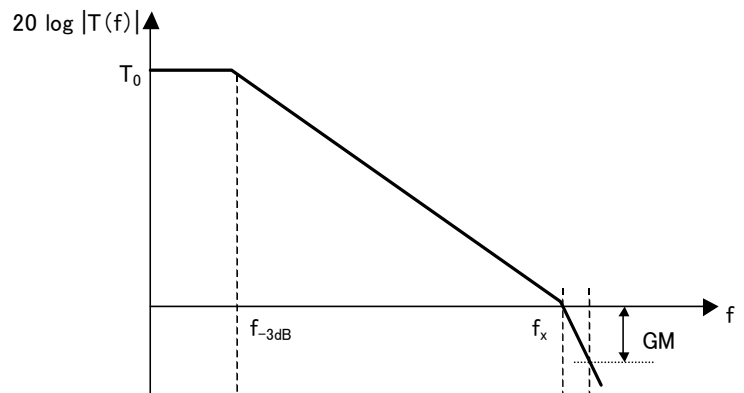
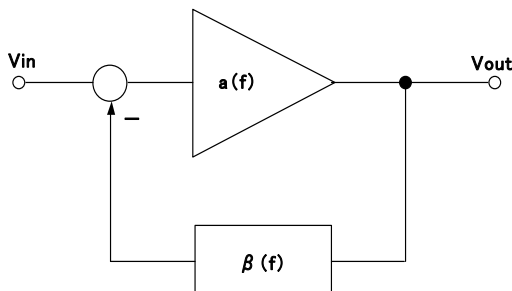
T(f) = β(f) a(f) is a parameter called loop gain, and is determined by the product of amplification factor and feedback factor of amplifier. As can be seen from the equation (3.12.2), as long as the loop gain is great, the gain of system in general (transmission function) is 1/β(f). When the phase of T(f) rotates 180 degrees and the magnitude is 1, then V_{out}/V_{in} = ∞ in the equation (3.12.1), and V is output even when input is zero. It means oscillation. In order to make negative feedback circuit stable, before the phase of loop gain rotates 180 degrees, its magnitude must be attenuated below 1. Stable condition is shown in the equation below:

$$\text{Stable condition of negative feedback system } |T(f)| < 1, \angle T(f) = 180 \tag{3.12.4}$$

Figure 3.12.1 shows an example of frequency characteristics of loop gain. Indicator for determining the stability of negative feedback system includes phase margin φ_m and gain margin GM.

$$\phi_m = 180^\circ - |\angle T(f_x)| \tag{3.12.5}$$

$$GM = 20 \log (1 / |T(f-180^\circ)|) \tag{3.12.6}$$



Negative feedback system is constructed below relationship
 $a(f) \cdot (V_{in} - \beta(f) \cdot V_{out}) = V_{out}$

transfer function A(f) is
 $A(f) = V_{out}/V_{in} = a(f) / (1 + a(f) \cdot \beta(f))$
 $= a(f) / (1 + T(f))$
 $= (1 / \beta(f)) \cdot (1 + 1/T(f))^{-1}$

where, T(f) = a(f) · β(f) is loop gain
 If loop gain is satisfied T(f) >> 1,
 transfer function is A(f) ≅ 1/β(f)

(a) Model of negative feedback system

(b) Loop gain frequency response

Fig. 3.12.1 Negative feedback system model and loop gain frequency response

3.12.2 Stability of non-inverting amplifier and differentiator

Take an example of non-inverting amplifier and differentiator to consider stability. Feedback factor of non-inversion amplifier is determined by resistance, and does not depend on frequency. Flow of signal in feedback circuit is in the direction from output to input, therefore the feedback factor, loop gain, and transfer function are represented by the equation below:

$$\beta = V_{in-} / V_{out} = R1 / (R1 + R2) \tag{3.12.7}$$

$$T(f) = a(f) \cdot \beta = (a_0 / (1 + j \cdot (f / f_{-3dB}))) \cdot (R1 / (R1 + R2)) \tag{3.12.8}$$

$$A(f) = (1 / \beta) \cdot (1 + 1 / T(f))^{-1} \tag{3.12.9}$$

Gain $a(f)$ of op-amp alone and $1/\beta$ are shown in the bode plot in figure 3.12.2. On this bode plot, $T(f)$ is a difference between $a(f)$ and $1/\beta$. ($20 \log |a(f)| - 20 \log |1/\beta| = 20 \log |a(f) \cdot \beta| = 20 \log |T(f)|$) The smaller β is (feedback amount smaller), the less is the delay of phase when $|T(f)| = 1$. The greater β is (feedback amount greater), the poorer is the stability. When $\beta = 1$, the smallest is the phase margin. $\beta = 1$ ($R1 = \infty, R2 = 0$) when voltage follower is configured, and stability of op-amp alone is required. Op-amp containing phase compensation capacitor in general is designed not to oscillate when voltage follower is configured. Figure 3.12.3 shows a differentiator (high pass filter).

In differentiator, feedback circuit contains capacitor, which delays the phase of loop gain. Stability can be improved by connecting a resistor in series to the capacitor. Feedback factor, loop gain, and transfer function are represented by the equation below:

$$\beta(f) = V_{in-} / V_{out} = (1 + j \cdot 2\pi f \cdot C1 R_s) / (1 + j \cdot 2\pi f \cdot C1 (R1 + R_s)) \tag{3.12.10}$$

$$T(f) = a(f) \cdot \beta(f) = (a_0 / (1 + j \cdot (f / f_{-3dB}))) \cdot (1 + j \cdot 2\pi f \cdot C1 R_s) / (1 + j \cdot 2\pi f \cdot C1 (R1 + R_s)) \tag{3.12.11}$$

$$A(f) = -j \cdot 2\pi f \cdot C1 R1 / (1 + j \cdot 2\pi f \cdot C1 R_s) \cdot (1 + 1 / T(f))^{-1} \tag{3.12.12}$$

Here, it should be noted that the transfer function in DC does not follow $1/\beta(0)$ when inverting amplifier is configured, but equals to $-(R1/R_s + 1/j \cdot 2\pi f \cdot C1)$. In a differentiator, it can be seen that the phase of loop gain advances and stability improves when R_s is connected to $C1$ in series.

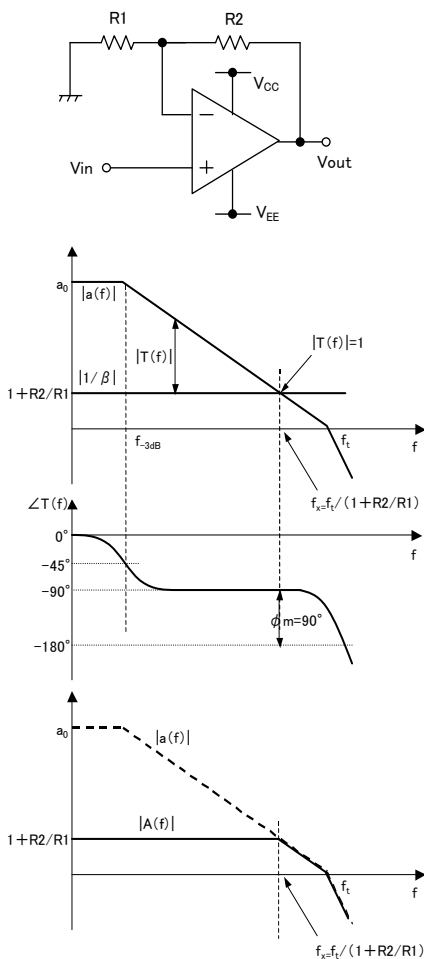


Fig. 3.12.2 loop gain frequency response of non-inverting amp

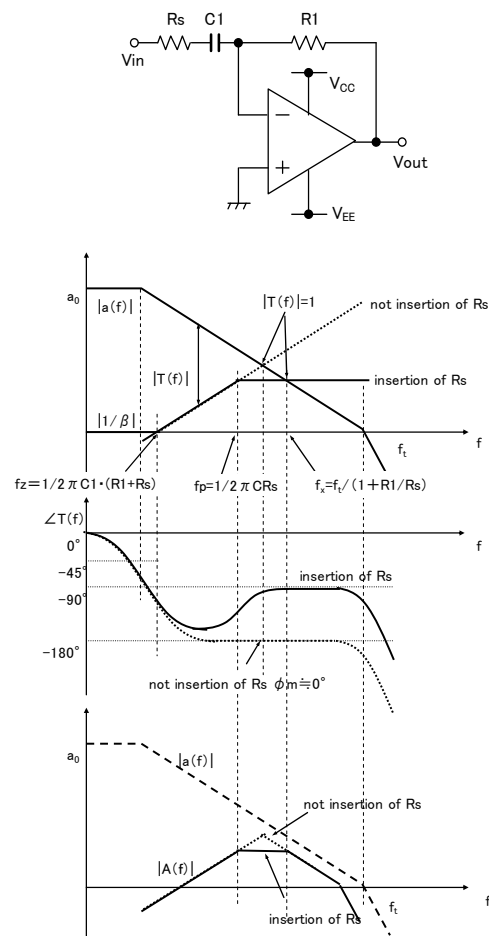


Fig.3.12.3 loop gain frequency response of differentiator

3.13 Total Harmonic Distortion plus Noise (THD + N)

It shows how much harmonic component and noise component are contained in output signal.

$$THD + N = (\text{Sum of harmonic component and noise component}) / (\text{Output voltage})$$

Harmonics is generated by nonlinearity of op-amp circuit. It results from the fact that the current - voltage static characteristic of transistor is exponential function (for bipolar transistor), and amplification factor is a nonlinear function with reference to input voltage, etc. Noise is generated not only by disturbance but also by peripheral components such as semiconductor element within IC and resistor. Output from op-amp contains these components, which distort the waveform.

When an amplifier is configured with op-amp, not only input signal but also noise component is amplified. Therefore, when a circuit with great amplification factor is configured, distortion factor becomes greater if output signal level is small.

Figure 3.13.2 (a) shows an example of output amplitude - frequency characteristics using the gain as a parameter. Output signal is limited by the slew rate of op-amp. Therefore, when a signal has a great frequency or when output signal has a great amplitude, distortion factor becomes great. Figure 3.13.2(b) shows a distortion factor characteristic using the signal frequency as a parameter.

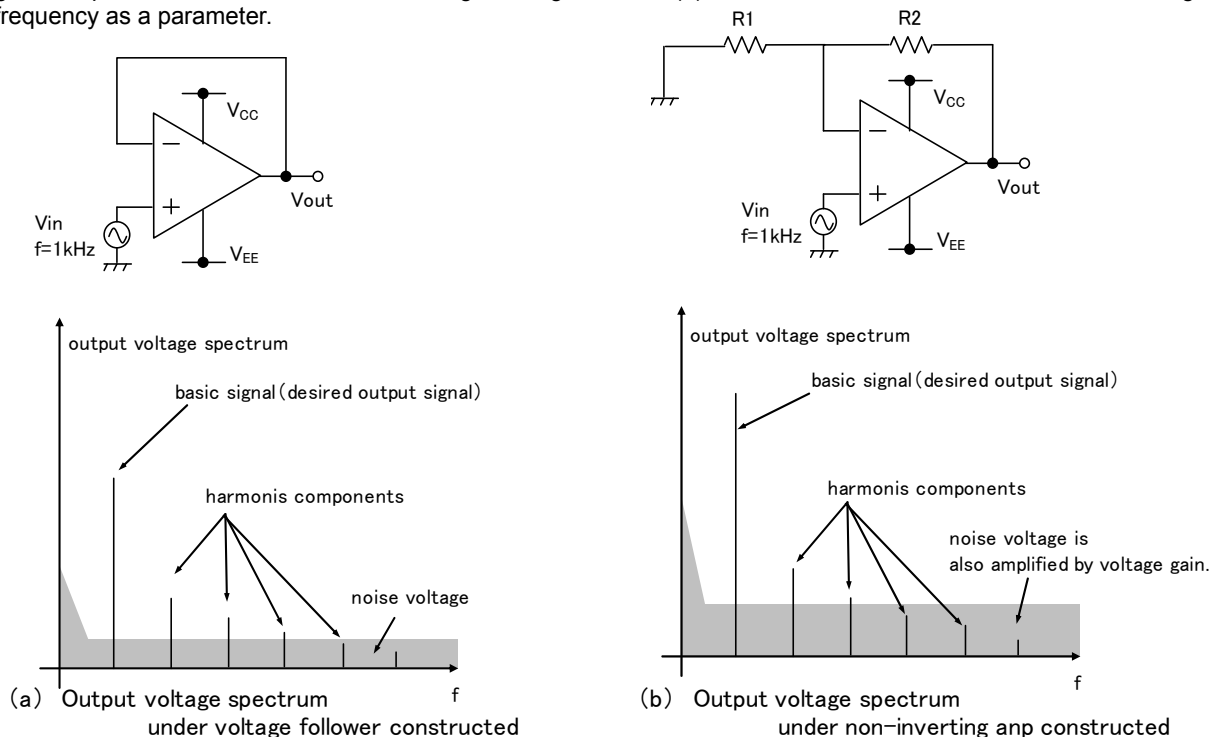


Fig. 3.13.1 Image of THD+N

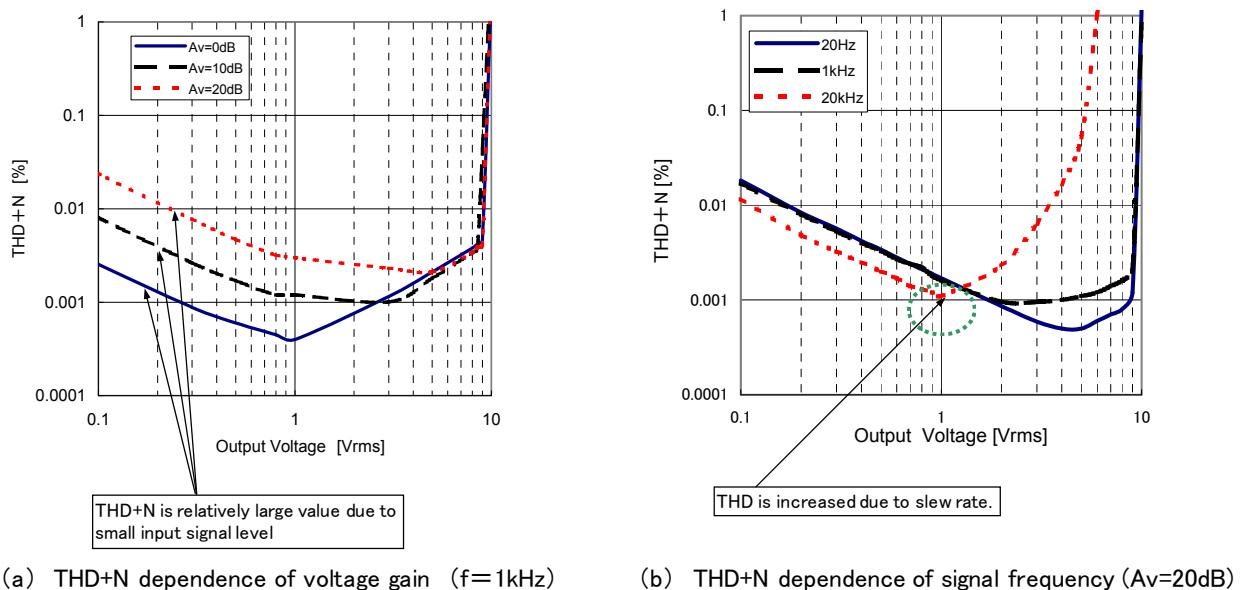


Fig. 3.13.2 BA4558R THD + N vs. output voltage (V+=15V,V--15V,RL=10kΩ,DIN AUDIO FILTER)

In addition, it is possible that the distortion factor becomes extremely high depending on output circuit configuration and load condition. Figure 3.13.3 shows the output circuit and distortion factor of op-amp of BA4558R and BA2904. BA4558R has an output circuit configuration called push-pull circuit of class AB. In this output circuit configuration, idling current is always allowed to flow in the output transistor to turn it on, which suppresses crossover distortion generated when source current and sink current are switched. BA2904 type has an output configuration called push-pull circuit of class C, and performs operation of class A when output sink current is small. When sink current exceeds several ten μA , great current PNP transistor Q4 turns on and crossover distortion is generated. Especially, when it is used by split power supplies, care should be taken because intake current may become great. This crossover distortion can be suppressed by always turning on PNPTr by use of pull-up resistor or by restricting intake current within several ten μA .

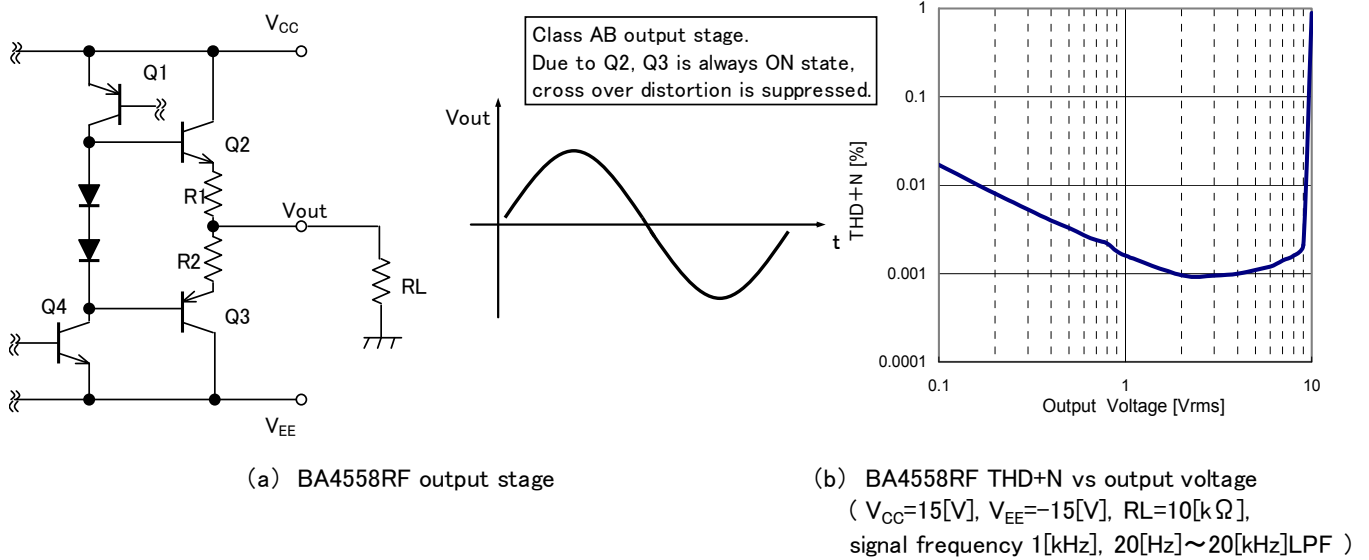


Fig. 3.13.3 BA4558RF output stage and THD+N

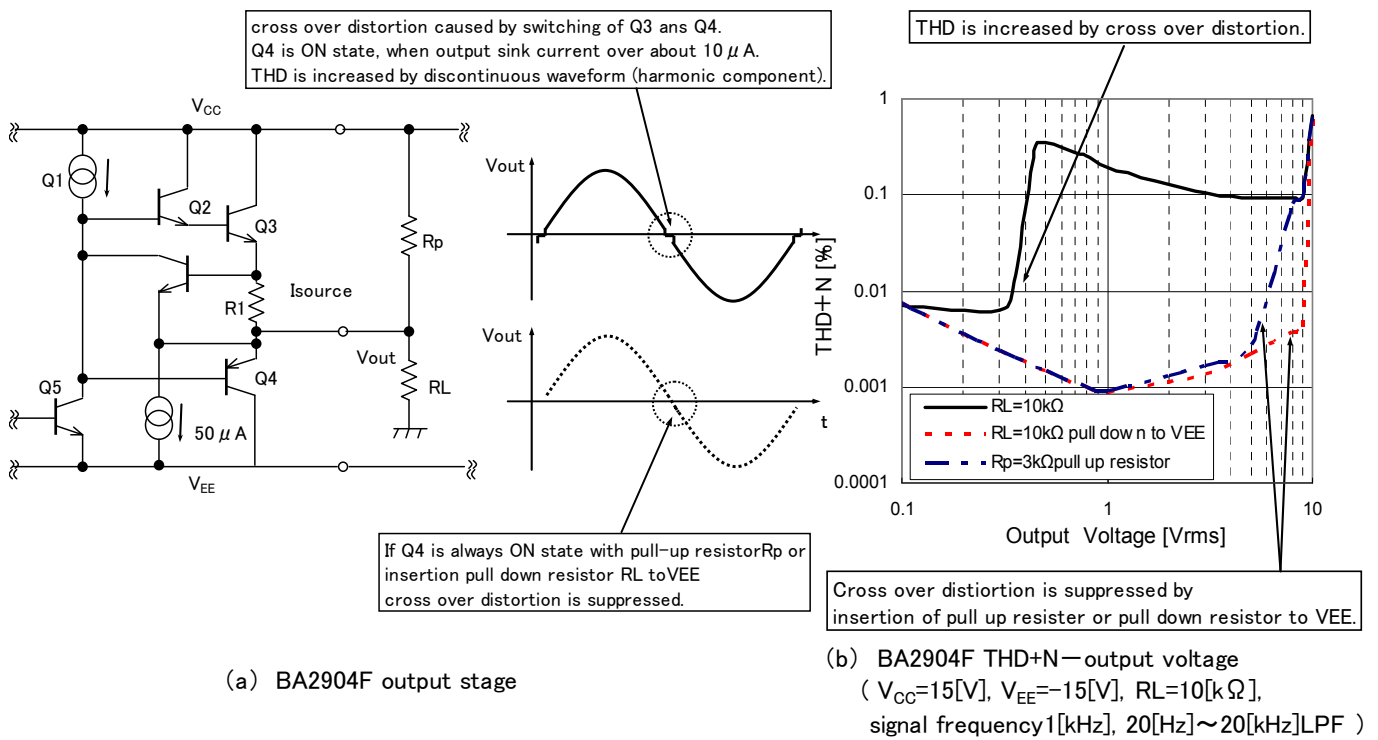


Fig. 3.13.4 BA2904F output stage and THD+N

3.14 Equivalent input noise source (input referred noise source)

Output noise from op-amp is converted into input noise voltage source, which makes an equivalent input noise source. equivalent input noise source is divided into input equivalent input noise voltage and equivalent input noise current. Noise contains a wide range of frequency component, and is normally represented by frequency spectrum. Noise is generated not only by disturbance, but also by chronologically discontinuous movement of electron. Noise generated by resistor and semiconductor element is mainly thermal noise, shot noise, and flicker noise (1/f noise). Principal mechanism by which noise is generated includes the following:

- Thermal noise : Thermal random movement of electron in resistor. Distributed in a wide range of frequency area (white noise).
Noise generated in resistor of resistance R is $V_{nr}^2/\Delta f = 4kTR$, $I_{nr}^2/\Delta f = 4kT/R$.
- Shot noise : Noise observed in active element, which is caused by electron passing depletion layer discontinuously (chronologically). It is found in forward current of diode, etc. Distributed in a wide range of frequency area (white noise).
When we put DC current flowing in active element at I, $I_n^2/\Delta f = 2qI$ is established.
- Flicker noise : Noise observed in active element, which is caused when trap generated by crystal defect captures and emits electron at random. Noise distributed in low-frequency area. It is also called 1/f noise because noise power density is inversely proportional to frequency. It is considered to be caused by crystal defect between base and emitter of bipolar transistor. When we put DC current flowing in element at I (base current as for bipolar transistor), $I_n^2/\Delta f = k I_a / f$ is established.
Where, k: Boltzmann constant, T: absolute temperature, K and a: constant determined by process, and Δf : frequency range which is interested in.

Op-amp consists of passive element such as resistor and active element such as transistor, and emits noise. The model of op-amp including equivalent input noise source is shown in figure 3.14.1. Noise has no polarity, and input noise source must be considered on both + input voltage and - input voltage. Considering that op-amp amplifies the difference between + input voltage and - input voltage, input conversion noise voltage can be collected either on + input terminal or - input terminal.

Normally, equivalent input noise voltage is considered on + input terminal side. Consider the processing input terminal for the reason for considering both noise voltage and noise current. Noise appears on output even when input terminal is shorted or opened with no input signal applied to op-amp. When input terminal is shorted, input noise current source can be ignored, so that output noise is generated from input noise voltage source. When high resistance is connected to the input terminal, the input noise current source generates a great voltage fall and is amplified and output, so that output noise is dominantly affected by input noise current source.

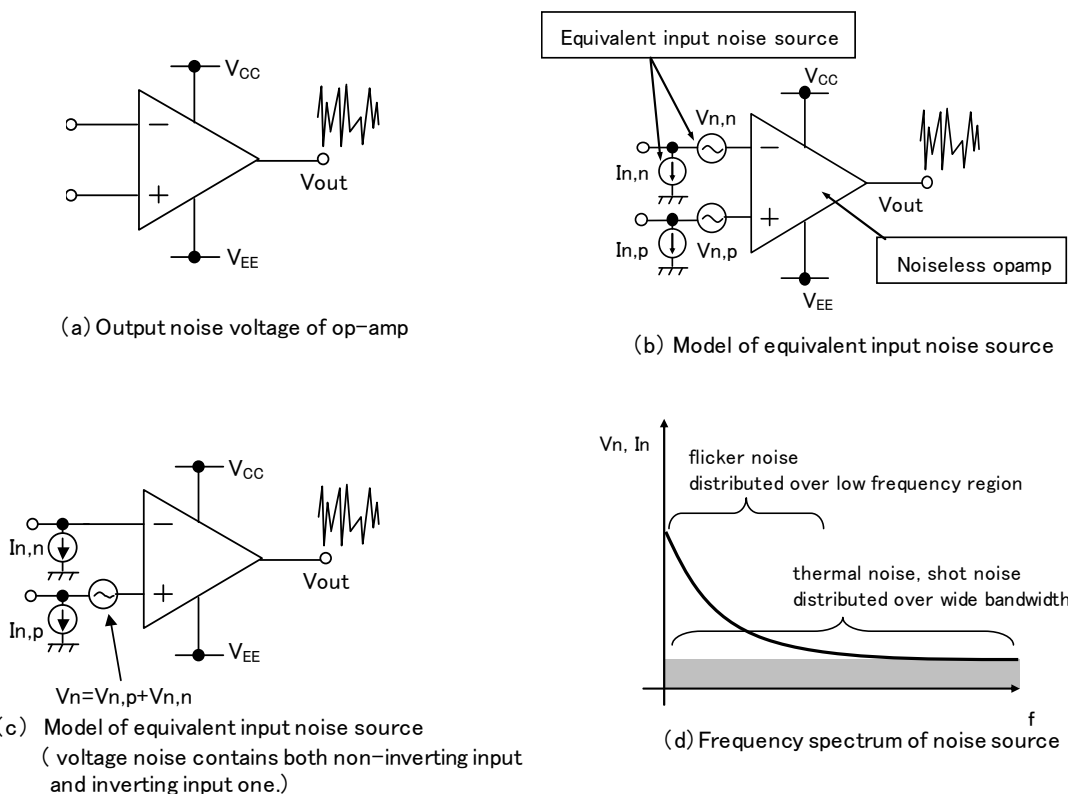


Fig. 3.14.1 Noise source model of op-amp

Consider the output noise voltage on non-inverting amplifier in figure 3.14.2. Put the thermal noise generated from resistor R1, R2, and R3 respectively at In1, In2, and In3. It is impossible to superimpose voltage and amperage on noise, but it is possible to superimpose by power. When we convert all noise sources as equivalent input noise voltage source Vnt, it is as follows:

$$Vnt^2 = Vni^2 + R3^2 \cdot (In3^2 + Inp^2) + (R1 // R2)^2 \cdot (Inn^2 + In1^2 + In2^2) \tag{3.13.1}$$

$$= Vni^2 + R3^2 \cdot Inp^2 + (R1 // R2)^2 \cdot Inn^2 + 4kT \cdot \{R3 + (R1 // R2)\} \tag{3.13.2}$$

$$= Vni^2 + \{R3^2 + (R1 // R2)^2\} \cdot In^2 + 4kT \cdot \{R3 + (R1 // R2)\} \text{ (assuming } Inp = Inn) \tag{3.13.3}$$

where, $Vni^2 = Vnw^2 \cdot (fcv/f + 1)$, $In^2 = Inw^2 \cdot (fci/f + 1)$, Boltzmann's constant k, fcv , fci is the corner frequency of noise voltage and noise current, respectively. (Fig 3.13.2(c))

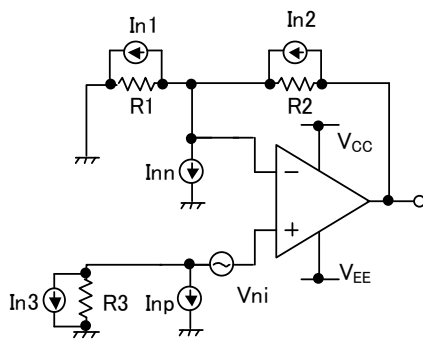
The voltage gain of non-inverting amplifier is represented A(f), output noise voltage is following,

$$Vno = \{ \int |A(f)|^2 \cdot Vnt^2 df \}^{1/2}$$

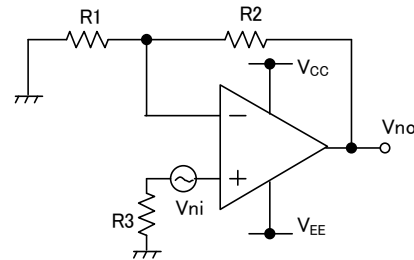
If non-inverting amplifier is assumed one order integrator, that is $A(f) = A0 / (1 + j \cdot f / fa)$, output voltage noise within frequency bandwidth fL to fH is approximated bellow equation.

$$Vno = (1 + R2/R1) \cdot \{ Vnw^2 \cdot (fcv \cdot \log(fA/fL) + 1.57fA - fL) + (R3 + (R1//R2))^2 \cdot In^2 \cdot (fcv \cdot \log(fA/fL) + 1.57fA - fL) + 4kT \cdot (R3 + (R1//R2)) \cdot (1.57fA - fL) \}^{1/2} \tag{3.13.4}$$

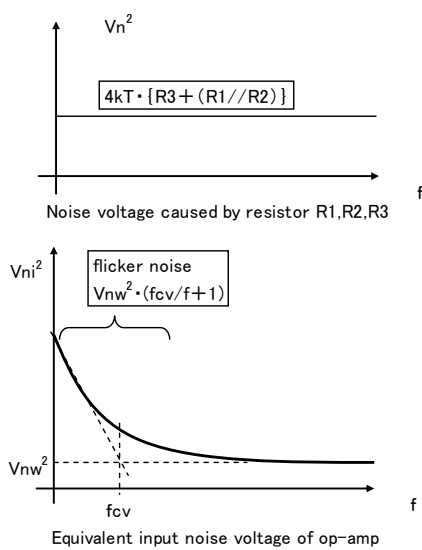
Fig.3.14.3(a), (b) is specified equivalent input noise voltage characteristics examples.



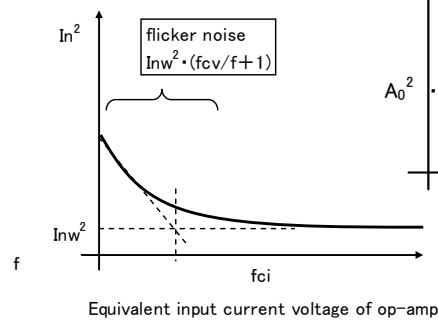
(a) noise source of non-inverting amplifier



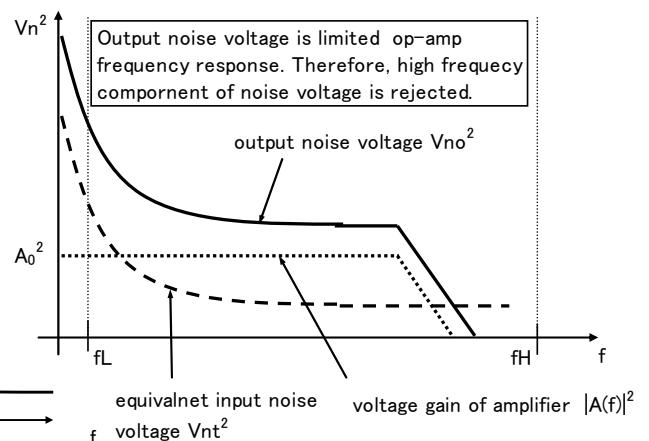
(b) equivalent input noise voltage of (a)



(c) component of equivalent input noise

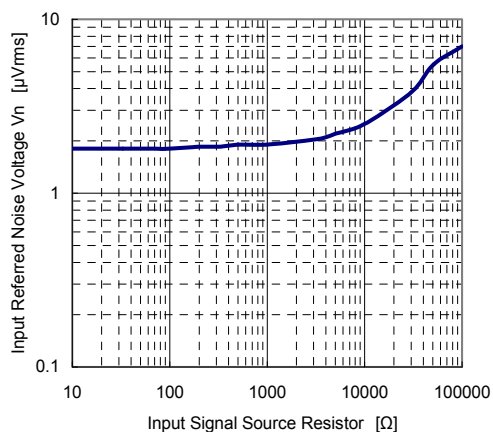
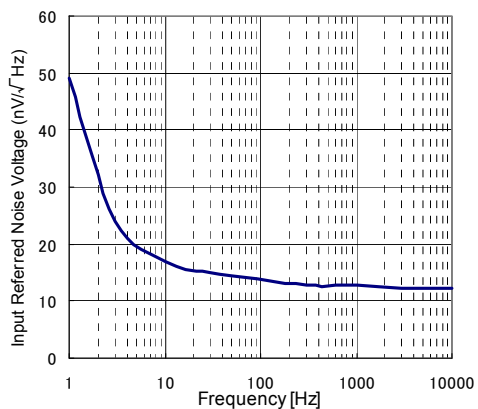


Equivalent input current noise of op-amp



(d) output noise voltage

Fig. 3.14.2 noise effect for non-inverting amplifier



(a) BA4558R equivalent input noise voltage vs. frequency ($V_{CC}=15V, V_{EE}=-15V, 20dB$ non-inverting amp) (b) BA4558R equivalent input noise voltage vs. signal source resistance ($V_{CC}=15V, V_{EE}=-15V, 20dB$ non-inverting amp, $20Hz \sim 20kHz$ LPF)

Fig. 3.14.3 Example of equivalent input noise spectrum

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.



Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

<http://www.rohm.com/contact/>