STRUCTURE Silicon monolithic integrated circuit

PRODUCT NAME BU9794KV

FUNCTION LCD control driver for segment type LCD display

FEATURE

- ○ LCD drive output : Common output : 4, Segment output : 50
- ○ built-in Display Data RAM (DDRAM): 50*4=200 bit
- ○ 3-wire Serial Interface (SD, SCL, SCB)
- ○ On chip oscillator circuit
- ○ LCD driver power-supply circuit:
  1/2, 1/3Bias, 1/4Duty, On chip Buffer AMP
- ○ No external component
- ○ Low power consumption design
- ○ support standby mode
- ○ Support blink function
- ○ Driver power supply: 2.5V～5.5V
- ○ LCD driving power supply: 2.5～5.5V

○ **Absolute maximum ratings (VSS = 0V)**

Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage 1	VDD	-0.5 ～ +7.0	V	Power supply
Power supply voltage 2	VLCD	-0.5 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	0.75*1	W	
Input voltage range	VIN	-0.5 ～ VDD+0.5	V	
Operational temperature range	Topr	-40 ～ +85	℃	
Storage temperature range	Tstg	-55 ～ +125	℃	

*1 When use more than Ta=25℃, subtract 7.5mW per degree.

○ **Recommend operating conditions (Ta = 25℃, VSS = 0V)**

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power supply voltage 1	VDD	2.5	-	5.5	V	Power supply
Power supply voltage 2	VLCD	2.5	-	5.5	V	LCD drive voltage

Note: Please use in VLCD≧VDD condition.

◎ This product is not designed against radioactive ray.

- ● **As for contents of mention of these materials. A service in the foreign exchange and foreign trade control law (Technology in the design, the manufacture and the use). Be careful of handling because it is likely to correspond.**
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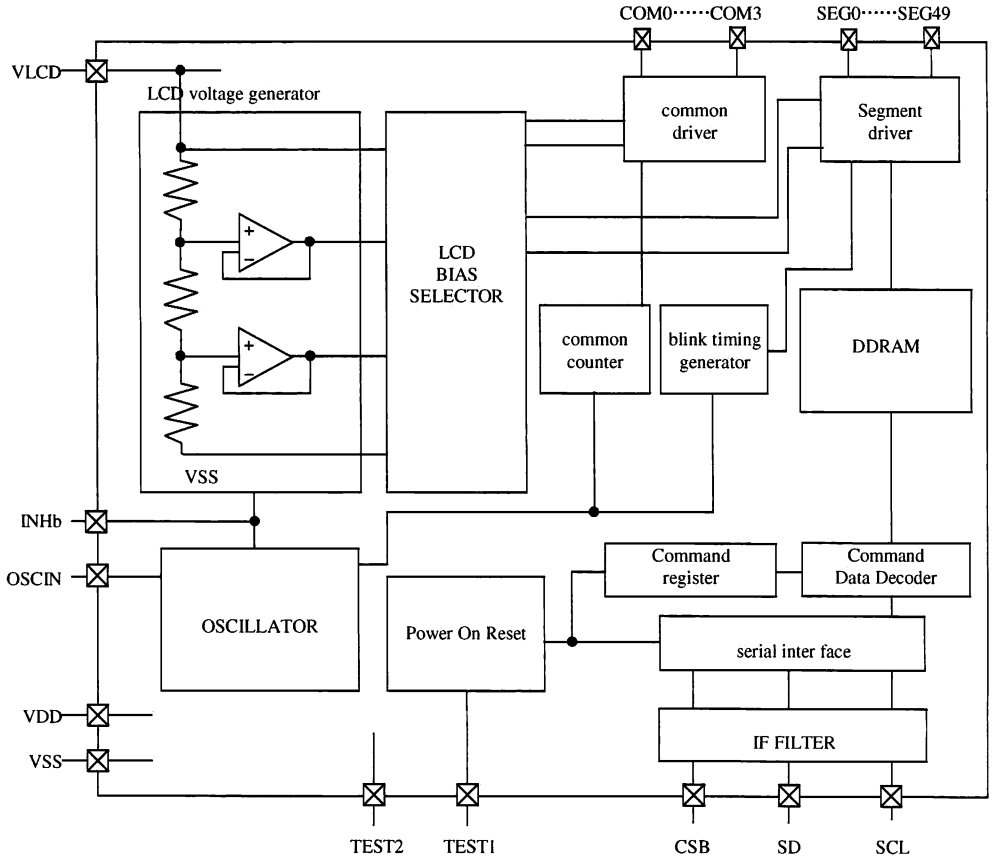
Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

○ Block diagrams



○ Electrical Characteristics

DC Characteristics (VDD=2.5～5.5V, VSS=0V, VLCD=2.5～5.5V, Ta=-40～85℃; unless otherwise specified)

Parameter		Symbol	Limit			Unit	Condition
			MIN	TYP	MAX		
"H" level input voltage		VIH	0.8VDD	-	VDD	V	SCL,CSB,SD
"L" level input voltage		VIL	VSS	-	0.2VDD	V	SCL,CSB,SD
"H" level input current		IIH	-	-	1	uA	SCL,CSB,SD
"L" level input current		IIL	-1	-	-	uA	SCL,CSB,SD
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10uA
	COM	RON	-	3.5	-	kΩ	
Standby current		Ist	-	-	5	uA	Display off, Oscillation off
Power consumption1		IDD	-	5	15	uA	VDD=3.3V, VLCD=5V, Ta=25℃ Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption2		ILCD	-	10	20	uA	VDD=3.3V, VLCD=5V, Ta=25℃ Power save mode1, FR=70Hz 1/3 bias, Frame inverse

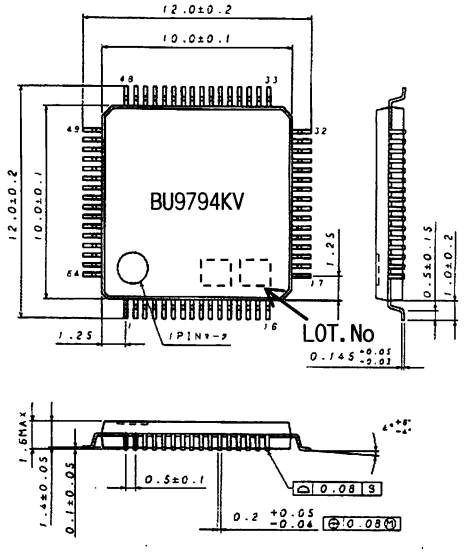
Oscillation Characteristics (Ta=-40～85℃, VDD=2.5～5.5V, VSS=0V unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Frame frequency	fCLK	68	80	92	Hz	FR = 80Hz setting VDD=3.3V

MPU interface Characteristics (Ta=-40～85℃, VDD=2.5V～5.5V, VLCD=2.0～5.5V, VSS=0V)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCYC	400	-	-	ns	
"H" SCL pulse width	tSHW	100	-	-	ns	
"L" SCL pulse width	tSLW	100	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
"H" CSB pulse width	tCHW	50	-	-	ns	

○ Outline drawing



Unit[mm]

Package: VQFP64

○ Terminal number/name

1	VLCD	9	TEST1	17	SEG6	25	SEG14	33	SEG22	41	SEG30	49	SEG38	57	SEG46
2	VDD	10	TEST2	18	SEG7	26	SEG15	34	SEG23	42	SEG31	50	SEG39	58	SEG47
3	VSS	11	SEG0	19	SEG8	27	SEG16	35	SEG24	43	SEG32	51	SEG40	59	SEG48
4	OSCIO	12	SEG1	20	SEG9	28	SEG17	36	SEG25	44	SEG33	52	SEG41	60	SEG49
5	CSB	13	SEG2	21	SEG10	29	SEG18	37	SEG26	45	SEG34	53	SEG42	61	COM0
6	SCL	14	SEG3	22	SEG11	30	SEG19	38	SEG27	46	SEG35	54	SEG43	62	COM1
7	SD	15	SEG4	23	SEG12	31	SEG20	39	SEG28	47	SEG36	55	SEG44	63	COM2
8	INHb	16	SEG5	24	SEG13	32	SEG21	40	SEG29	48	SEG37	56	SEG45	64	COM3

Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

Notes

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