

- ◇STRUCTURE Silicon Monolithic Integrated Circuit
- ◇PRODUCT 2048 × 8 bit Electrically Erasable PROM
- ◇PART NUMBER BU9844GUL-W
- ◇PHYSICAL DIMENSION Fig.-1
- ◇BLOCK DIAGRAM Fig.-2
- ◇USE General purpose
- ◇FEATURES
 - 2048 words × 8 bits architecture serial EEPROM
 - Wide operating voltage range (1.7V~5.5V)
 - Two wire serial interface
 - Self-timed write cycle with automatic erase
 - 16 byte Page Write mode
 - Low power consumption
 - Write (5V) : 1.2mA (Typ.)
 - Read (5V) : 0.2mA (Typ.)
 - Standby (5V) : 0.1 μA(Typ.)
 - DATA security
 - Write protect feature (WP pin)
 - Inhibit to WRITE at low Vcc
 - WLCSP package ----- VCSP50L1
 - High reliability fine pattern CMOS technology
 - Endurance : 1,000,000 erase/write cycles
 - Data retention : 40 years
 - Filtered inputs in SCL•SDA for noise suppression
 - Initial data FFh in all address

◇ ABSOLUTE MAXIMUM RATING (Ta=25°C)

| Parameter | Symbol | Rating | | Unit |
|-----------------------|--------|--------------|-----|------|
| Supply Voltage | Vcc | -0.3~6.5 | | V |
| Power Dissipation | Pd | VCSP50L1 | 220 | mW |
| Storage Temperature | Tstg | -65~125 | | °C |
| Operating Temperature | Topr | -40~85 | | °C |
| Terminal Voltage | — | -0.3~Vcc+0.3 | | V |

* Degradation is done at 2.2mW/°C for operation above 25°C

◇RECOMMENDED OPERATING CONDITION

| Parameter | Symbol | Rating | Unit |
|----------------|-----------------|-------------------|------|
| Supply Voltage | V _{CC} | 1.7~5.5 | V |
| Input Voltage | V _{IN} | 0~V _{CC} | V |

◇DC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=-40~85°C, V_{CC}=1.7~5.5V)

| Parameter | Symbol | Specification | | | Unit | test condition |
|------------------------|------------------|--------------------|------|--------------------|------|---|
| | | Min. | Typ. | Max. | | |
| “H” Input Voltage1 | V _{IH1} | 0.7V _{CC} | — | — | V | 2.5V ≤ V _{CC} ≤ 5.5V |
| “L” Input Voltage1 | V _{IL1} | — | — | 0.3V _{CC} | V | 2.5V ≤ V _{CC} ≤ 5.5V |
| “H” Input Voltage2 | V _{IH2} | 0.9V _{CC} | — | — | V | 1.7V ≤ V _{CC} < 2.5V |
| “L” Input Voltage2 | V _{IL2} | — | — | 0.1V _{CC} | V | 1.7V ≤ V _{CC} < 2.5V |
| “L” Output Voltage1 | V _{OL1} | — | — | 0.3 | V | I _{OL} =3.0mA, 2.5V ≤ V _{CC} ≤ 5.5V (SDA) |
| “L” Output Voltage2 | V _{OL2} | — | — | 0.2 | V | I _{OL} =1.5mA, 1.7V ≤ V _{CC} < 2.5V (SDA) |
| Input Leakage Current | I _{LI} | -1 | — | 1 | μA | V _{IN} =0V~V _{CC} |
| Output Leakage Current | I _{LO} | -1 | — | 1 | μA | V _{OUT} =0V~V _{CC} (SDA) |
| Operating Current | I _{CC1} | — | — | 2.0 | mA | V _{CC} =5.5V, f _{SCL} =400kHz, t _{WR} =5ms Byte Write Page Write |
| | I _{CC2} | — | — | 0.5 | mA | V _{CC} =5.5V, f _{SCL} =400kHz Random Read Current Read Sequential Read |
| Standby Current | I _{SB} | — | — | 2.0 | μA | V _{CC} =5.5V, SDA·SCL=V _{CC} A2=GND, WP=GND |

○ This product is not designed for protection against radioactive rays.

◇MEMORY CELL CHARACTERISTICS(Ta=25°C, V_{CC}=1.7~5.5V)

| Parameter | Specification | | | Unit |
|-------------------|---------------|------|------|-------|
| | Min. | Typ. | Max. | |
| Write/Erase Cycle | 1,000,000 | — | — | cycle |
| Data Retention | 40 | — | — | year |

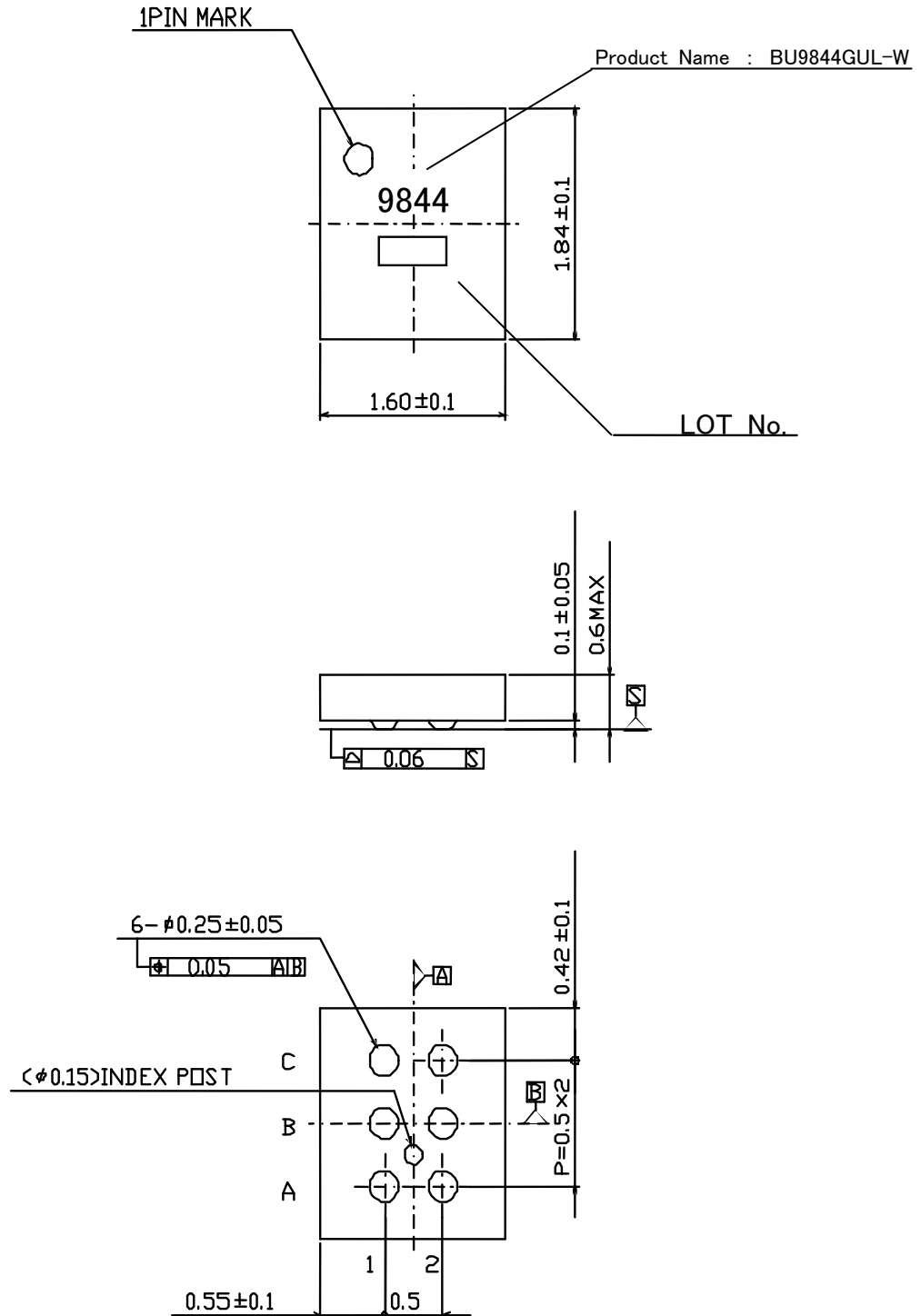


Fig.-1 PHYSICAL DIMENSION (VCSP50L1) (Unit : mm)

◇BLOCK DIAGRAM

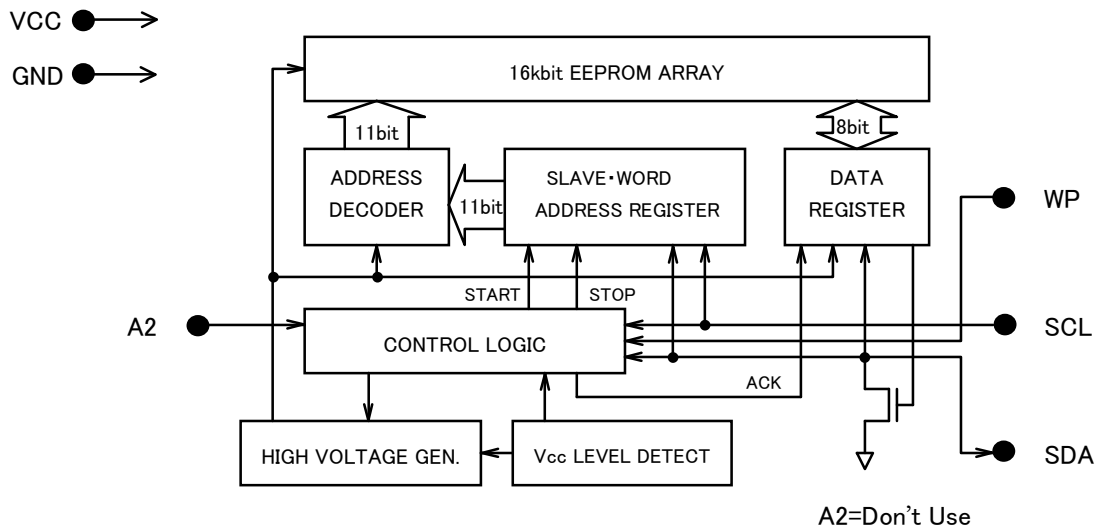


Fig.-2 BLOCK DIAGRAM

◇PIN CONFIGURATION

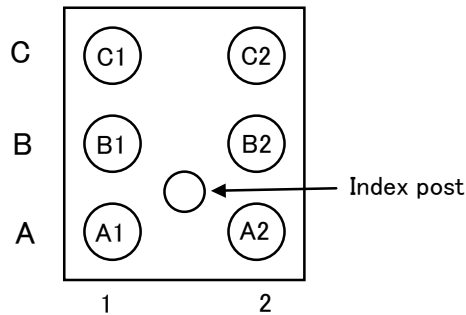


Fig.-3 BU9844GUL-W (bottom view)

◇PIN NAME

| Land No. | PIN NAME | I/O | FUNCTIONS |
|----------|----------|--------|--|
| A1 | VCC | — | Power Supply |
| A2 | A2 | IN | Out of Use (Vcc or GND or OPEN) |
| B1 | WP | IN | Write Protect Input |
| B2 | GND | IN | Ground (0V) |
| C1 | SCL | IN | Serial Clock Input |
| C2 | SDA | IN/OUT | Slave and Word Address, Serial Data Input, Serial Data Output *1 |

*1 An open drain output requires a pull-up resistor.

◇AC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=-40~85°C, Vcc=1.7~5.5V)

| Parameter | Symbol | FAST-MODE | | | STANDARD-MODE | | | Unit |
|---------------------------------|----------|------------------|------|------|------------------|------|------|------|
| | | 2.5 ≤ Vcc ≤ 5.5V | | | 1.7 ≤ Vcc ≤ 5.5V | | | |
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Clock Frequency | fSCL | — | — | 400 | — | — | 100 | kHz |
| Data Clock High Period | tHIGH | 0.6 | — | — | 4.0 | — | — | μs |
| Data Clock Low Period | tLOW | 1.2 | — | — | 4.7 | — | — | μs |
| SDA and SCL Rise Time | tR | — | — | 0.3 | — | — | 1.0 | μs |
| SDA and SCL Fall Time | tF | — | — | 0.3 | — | — | 0.3 | μs |
| Start Condition Hold Time | tHD:STA | 0.6 | — | — | 4.0 | — | — | μs |
| Start Condition Setup Time | tSU:STA | 0.6 | — | — | 4.7 | — | — | μs |
| Input Data Hold Time | tHD:DAT | 0 | — | — | 0 | — | — | ns |
| Input Data Setup Time | tSU:DAT | 100 | — | — | 250 | — | — | ns |
| Output Data Delay Time | tPD | 0.1 | — | 0.9 | 0.2 | — | 3.5 | μs |
| Output Data Hold Time | tDH | 0.1 | — | — | 0.2 | — | — | μs |
| Stop Condition Setup Time | tSU:STO | 0.6 | — | — | 4.7 | — | — | μs |
| Bus Free Time | tBUF | 1.2 | — | — | 4.7 | — | — | μs |
| Write Cycle Time | tWR | — | — | 5 | — | — | 5 | ms |
| Noise Spike Width (SDA and SCL) | tI | — | — | 0.1 | — | — | 0.1 | μs |
| WP Hold Time | tHD:WP | 0 | — | — | 0 | — | — | ns |
| WP Setup Time | tSU:WP | 0.1 | — | — | 0.1 | — | — | μs |
| WP High Period | tHIGH:WP | 1.0 | — | — | 1.0 | — | — | μs |

◇SYNCHRONOUS DATA TIMING

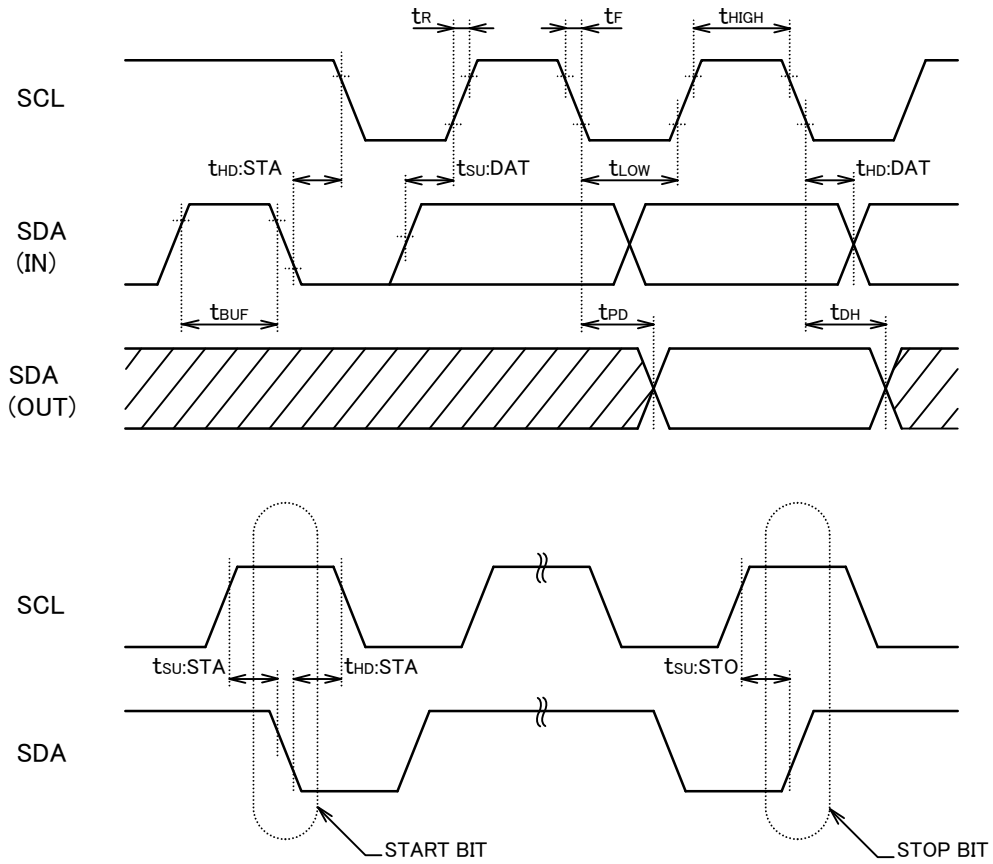


Fig.-4 SYNCHRONOUS DATA TIMING

- SDA data is latched into the chip at the rising edge of SCL clock.
- Output date toggles at the falling edge of SCL clock.

◇WRITE CYCLE TIMING

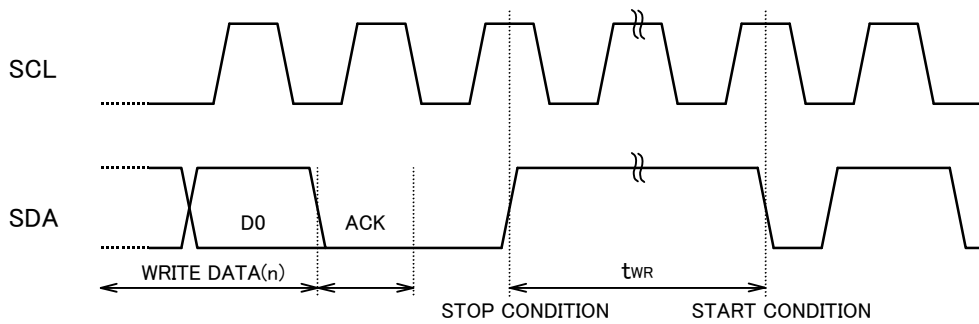


Fig.-5 WRITE CYCLE TIMING

◇WP TIMING

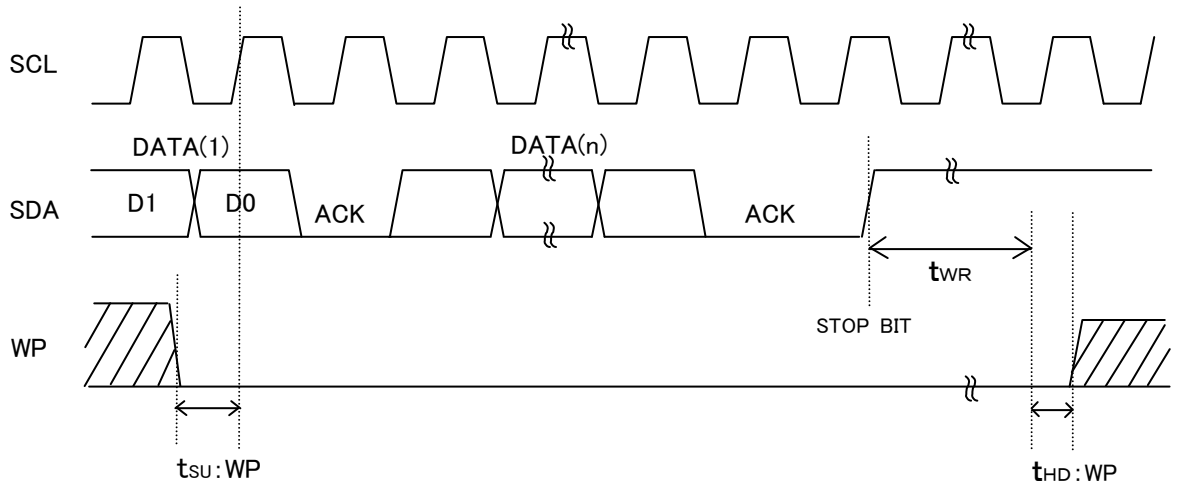


Fig.-6(a) WP TIMING OF THE WRITE OPERATION

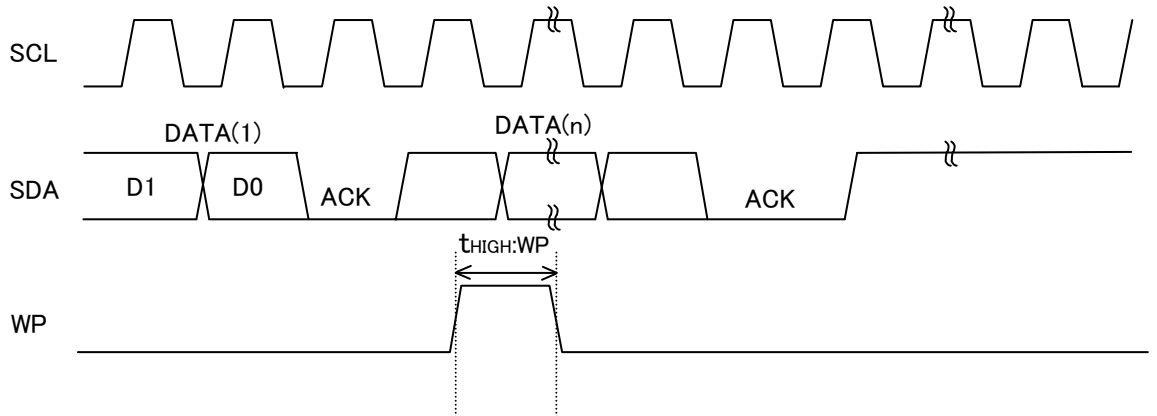


Fig.-6(b) WP TIMING OF THE WRITE CANCEL OPERATION

- For the WRITE operation, WP must be "LOW" during the period of time from the rising edge of the clock which takes in D0 of first byte until the end of t_{WR} . (See Fig.-6(a))
 During this period, WRITE operation is canceled by setting WP "HIGH".(See Fig.-6(b))
- In the case of setting WP "HIGH" during t_{WR} , WRITE operation is stopped in the middle and the data of accessing address is not guaranteed. Please write correct data again in the case.

◇DEVICE OPERATION

○START CONDITION (RECOGNITION OF START BIT)

- All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH.
- The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.
(See Fig.-4 SYNCHRONOUS DATA TIMING)

○STOP CONDITION (RECOGNITION OF STOP BIT)

- All commands must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.
(See Fig.-4 SYNCHRONOUS DATA TIMING)

○NOTICE ABOUT WRITE COMMAND

- In the case that stop condition is not excuted in WRITE mode, transfered data will not be written in a memory.

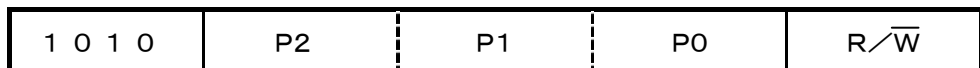
○DEVICE ADDRESSING

- Following a START condition, the master output the slave address to be accessed.
- The most significant four bits of the slave address are the “device type identifier,” for this device it is fixed as “1010.”
- The next three bits (P2,P1,P0) are used by the master to select eight 256 word page of memory.

P2,P1,P0 set to '0' '0' '0' . . . 1page(000~0FF)
 P2,P1,P0 set to '0' '0' '1' . . . 2page(100~1FF)
 .
 .
 .
 P2,P1,P0 set to '1' '1' '1' . . . 8page(700~7FF)

- The last bit of the stream ($\overline{R/W}$ ··· $\overline{READ/WRITE}$) determines the operation to be performed. When set to “1”, a read operation is selected ; when set to “0”, a write operation is selected.

$\overline{R/W}$ set to “0” ·········· WRITE (including word address input of Random Read)
 $\overline{R/W}$ set to “1” ·········· READ



○WRITE PROTECT (WP)

- When WP pin set to Vcc(H level), write protect is set for 2,048 words (all address).
- When WP pin set to GND(L level), it is enable to write 2,048 words (all address).
- Either control this pin or connect to GND (or Vcc). It is inhibited from being left unconnected.

○ACKNOWLEDGE

- Acknowledge is a software convention used to indicate successful data transfers. The transmitter device will release the bus after transmitting eight bits. (When inputting the slave address in the write or read operation, transmitter is μ -COM. When outputting the data in the read operation, it is this device.)
- During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that the eight bits of data has been received. (When inputting the slave address in the write or read operation, receiver is this device. When outputting the data in the read operation, it is μ -COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In the WRITE mode, the device will respond with an Acknowledge, after the receipt of each subsequent 8-bit word (word address and write data).
- In the READ mode, the device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected, and no STOP condition is generated by the master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode. (See Fig-7 ACKNOWLEDGE RESPONSE FROM RECEIVER)

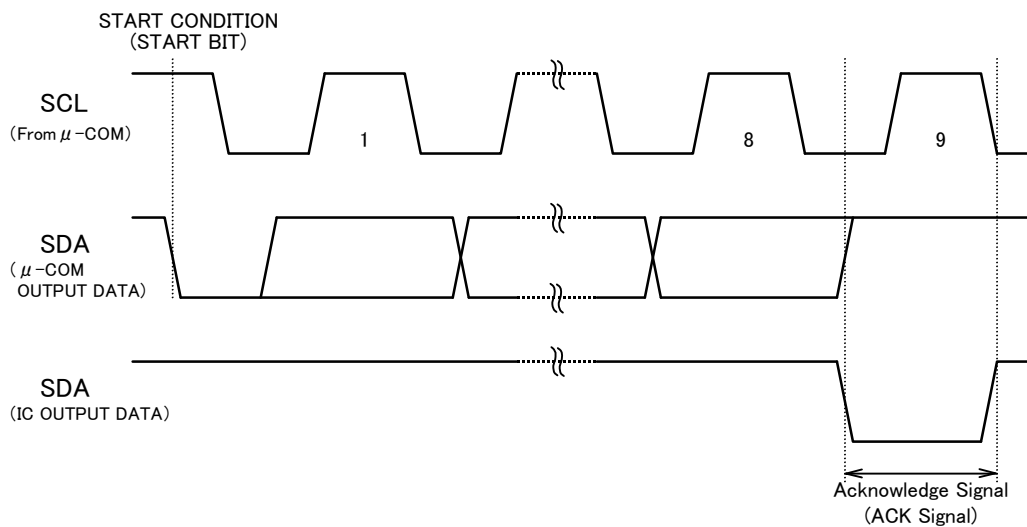


Fig.-7 ACKNOWLEDGE RESPONSE FROM RECEIVER

◇ BYTE WRITE

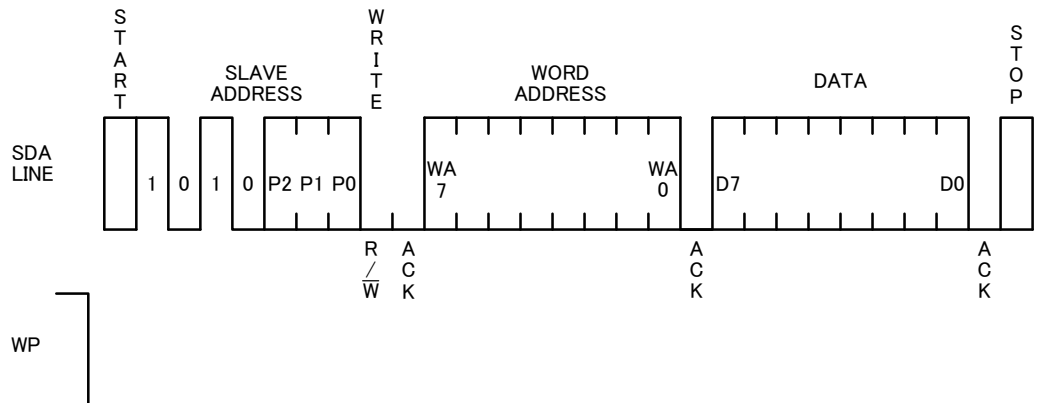


Fig.-8 BYTE WRITE CYCLE TIMING

- By using this command, the data is programmed into the indicated word address.
- When the master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.

◇ PAGE WRITE

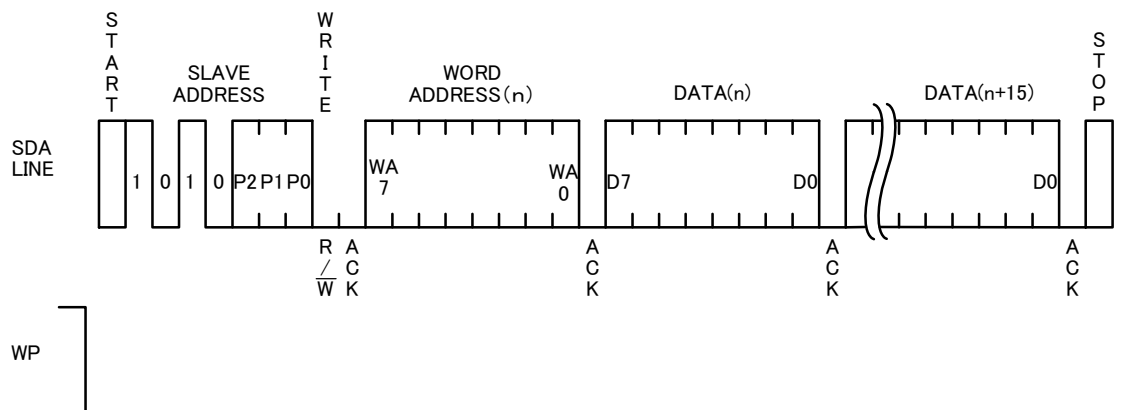


Fig.-9 PAGE WRITE CYCLE TIMING

- This device is capable of sixteen byte Page Write operation.
- When two or more byte data are inputted, the four low order address bits are internally incremented by one after the receipt of each word. The seven higher order bits of the address (P2~P0, WA7~WA4) remain constant.
- If the master transmits more than sixteen words, prior to generating the STOP condition, the address counter will “roll over,” and the previous transmitted data will be overwritten.

◇CURRENT READ

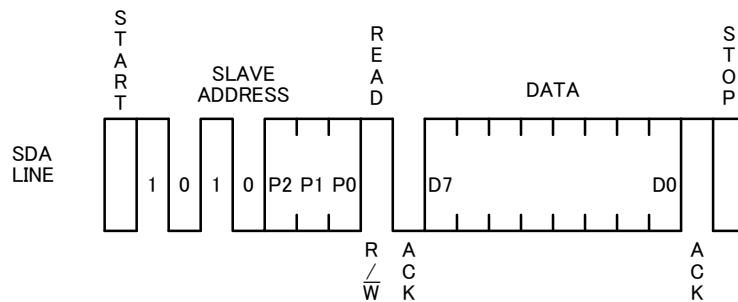


Fig.-10 CURRENT READ CYCLE TIMING

- In case that the previous operation is Random or Current Read (which includes Sequential Read respectively), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
If the last command is Byte or Page Write, the internal address counter stays at the last address (n). Thus Current Read outputs the data of the word address (n).
- If an Acknowledge is detected, and no STOP condition is generated by the master (μ -COM), the device will continue to transmit the data. [It can transmit all data (16kbit 2048word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

◇RANDOM READ

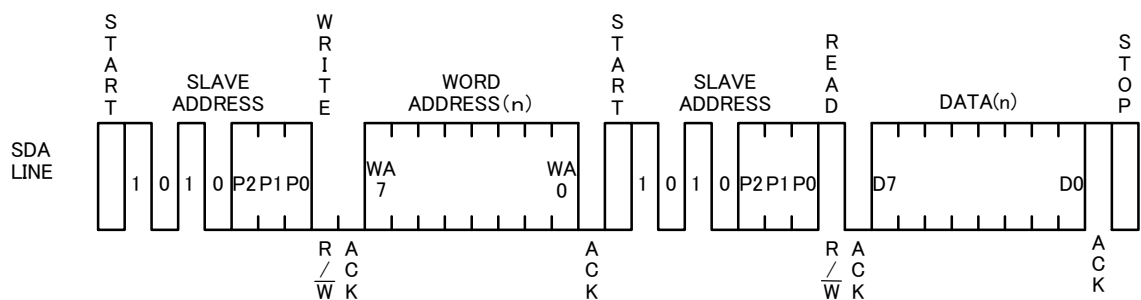


Fig.-11 RANDOM READ CYCLE TIMING

- Random Read operation allows the master to access any memory location indicated word address.
- If an Acknowledge is detected, and no STOP condition is generated by the master (μ -COM), the device will continue to transmit the data. [It can transmit all data (16kbit 2048word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

◇SEQUENTIAL READ

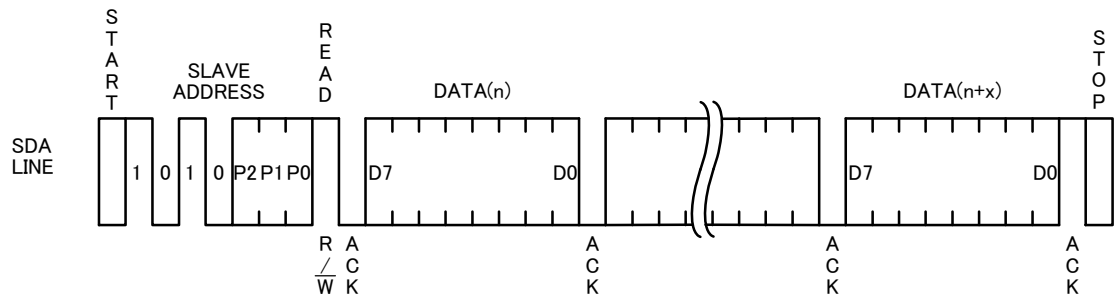


Fig.-12 SEQUENTIAL READ CYCLE TIMING
(Current Read)

- If an Acknowledge is detected, and no STOP condition is generated by the master (μ -COM), the device will continue to transmit the data. [It can transmit all data (16kbit 2048word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.
- The Sequential Read operation can be performed with both Current Read and Random Read.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

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