◇STRUCTURE Silicon Monolithic Integrated Circuit

◇PRODUCT 1,024×8 bit Electrically Erasable PROM

◇PART NUMBER BU9832GUL－W

◇PHYSICAL DIMENSION Fig.1 (Plastic Mold)

◇BLOCK DIAGRAM Fig.2

◇USE General purpose

◇FEATURES

・1,024 words × 8 bits architecture serial EEPROM
・Wide operating voltage range (1.8V～5.5V)
・Serial Peripheral Interface (CPOL,CPHA)=(0.0),(1.1)
・Self-timed write cycle with automatic erase
・Low power consumption
Write (5V) : 1.5mA (Typ.)
Read (5V) : 0.5mA (Typ.)
Standby (5V) : 0.1μA(Typ.)
・Auto-increment of registers address for Read mode
・32 byte Page Write mode
・DATA security
Defaults to power up with write-disabled state
Software instructions for write-enable/disable
Write status register protect feature (WPB pin)
Block writes protection by status register
Write inhibit at low VCC
・WL-CSP package ------ VCSP50L2
・High reliability fine pattern CMOS technology
・Initial data FFh in all address and 00h in status register
・Data retention : 40 years
・Endurance : 1,000,000 erase/write cycles

◇ ABSOLUTE MAXIMUM RATING (Ta=25℃)

Parameter	Symbol	Rating		Unit
Supply Voltage	VCC	−0.3～6.5		V
Power Dissipation	Pd	VCSP50L2	220	mW
Storage Temperature	Tstg	−65～125		℃
Operating Temperature	Topr	−40～85		℃
Terminal Voltage	—	−0.3～VCC+0.3		V

*Degradation is done at 2.2mW/℃ for operation above 25℃

◇RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	1.8～5.5	V
Input Voltage	V_{IN}	0～V_{CC}	V

◇DC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=−40～85℃、VCC=1.8～5.5V)

Parameter	Symbol	Specification			Unit	test condition
		Min.	Typ.	Max.		
"H" Input Voltage1	V_{IH1}	0.7×Vcc	—	Vcc+0.3	V	1.8V≦Vcc≦5.5V
"L" Input Voltage1	V_{IL1}	−0.3	—	0.3×Vcc	V	1.8V≦Vcc≦5.5V
"L" Output Voltage1	V_{OL1}	0	—	0.4	V	IOL=2.1mA, 2.5V≦Vcc≦5.5V
"L" Output Voltage2	V_{OL2}	0	—	0.2	V	IOL=100μA, 1.8V≦Vcc＜2.5V
"H" Output Voltage1	V_{OH1}	Vcc−0.5	—	Vcc	V	IOH=−0.4mA (2.5V≦Vcc≦5.5V)
"H" Output Voltage2	V_{OH2}	Vcc−0.2	—	Vcc	V	IOH=−100μA (1.8V≦Vcc＜2.5V)
Input Leakage Current	I_{LI}	−1	—	1	μA	VIN=0V～Vcc
Output Leakage Current	I_{LO}	−1	—	1	μA	VOUT=0V～Vcc, CSB=Vcc
Operating Current Write	I_{CC1}	—	—	1.0	mA	Vcc=1.8V, fSCK=2MHz, tE/W=5ms Byte Write, Page Write Write Status Register
	I_{CC2}	—	—	2.0	mA	Vcc=2.5V, fSCK=5MHz, tE/W=5ms Byte Write, Page Write Write Status Register
	I_{CC3}	—	—	3.0	mA	Vcc=5.5V, fSCK=5MHz, tE/W=5ms Byte Write, Page Write Write Status Register
Operating Current Read	I_{CC3}	—	—	1.5	mA	Vcc=2.5V, fSCK=5MHz Read, Read Status Register
	I_{CC4}	—	—	2.0	mA	Vcc=5.5V, fSCK=5MHz Read, Read Status Register
Standby Current	I_{SB}	—	—	2.0	μA	Vcc=5.5V, $\overline{CS}$=$\overline{HOLD}$=$\overline{WP}$=Vcc, SCK=SI=Vcc or GND, SO=OPEN

○This product is not designed for protection against radioactive rays.

◇MEMORY CELL CHARACTERISTICS(Ta=25℃、Vcc=1.8～5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write/Erase Cycle ※1	1,000,000	—	—	Cycle
Data Retention ※1	40	—	—	Year

◇Input/Output Capacitance (Ta=25℃ frequency=5MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance ※1	C_{IN}	V_{IN}=GND	−	8	pF
Output Capacitance ※1	C_{OUT}	V_{OUT}=GND	−	8	pF

※1:Not 100% Tested

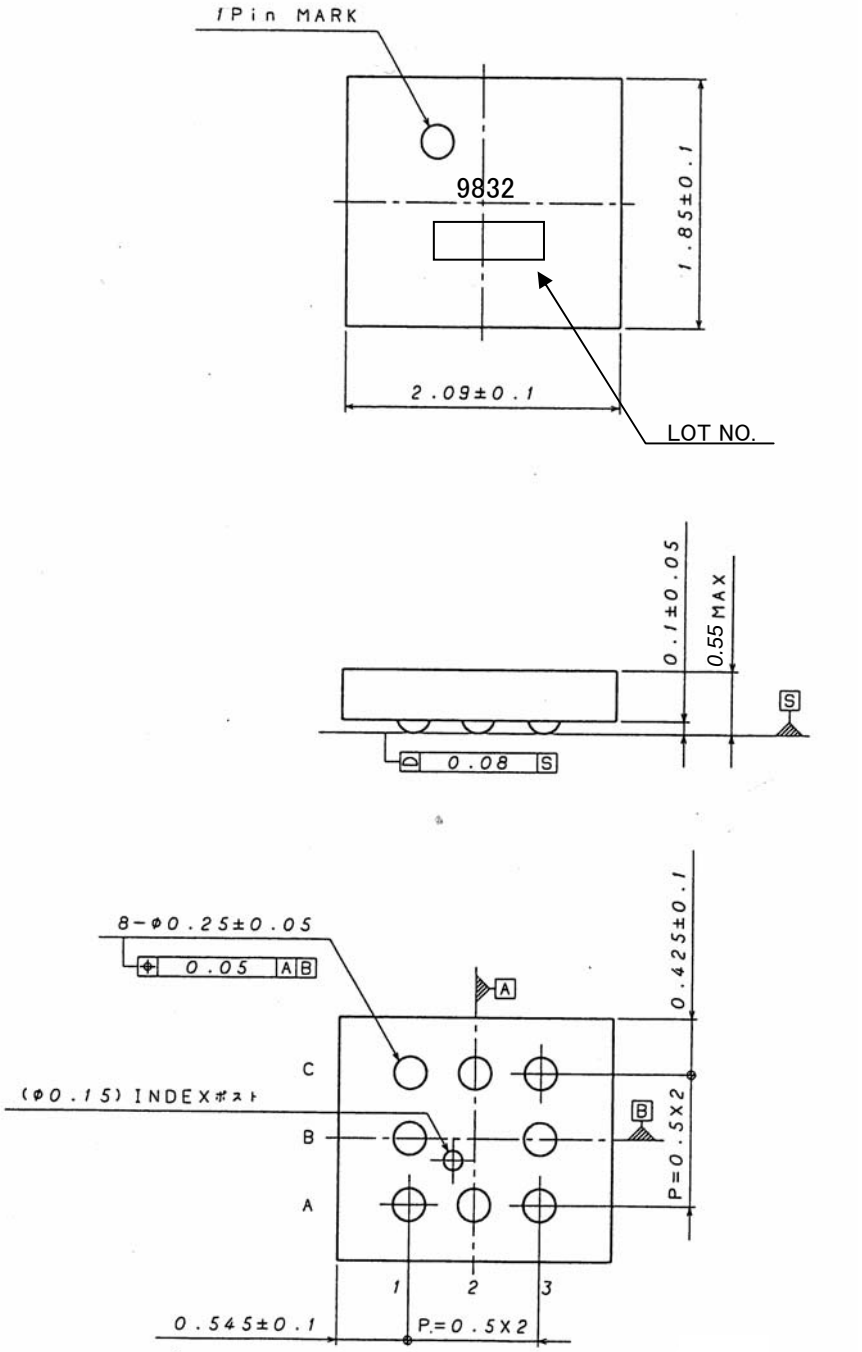

Fig.1 PHYSICAL DIMENSION

◇PIN CONFIGURATION

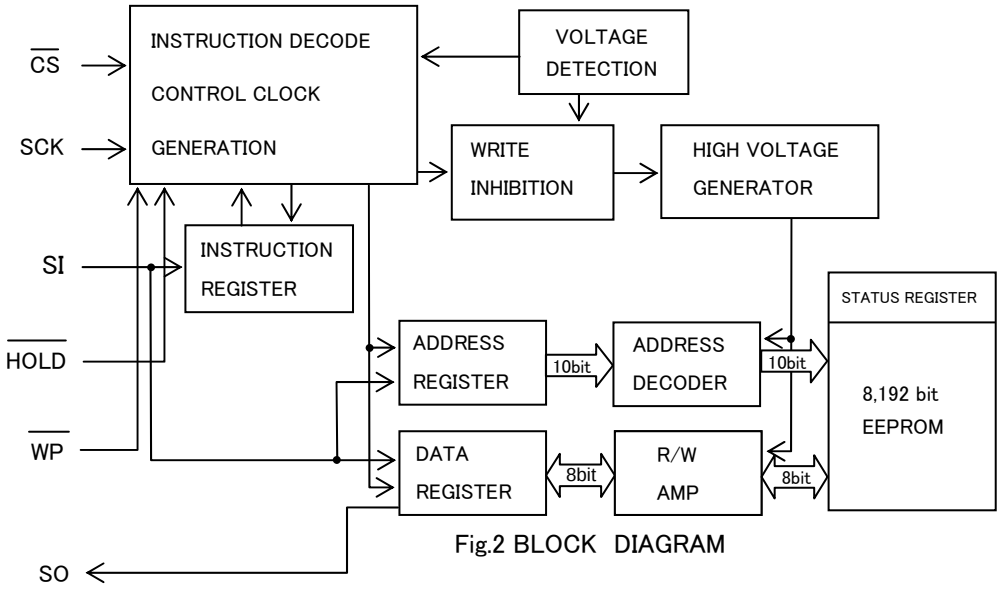

Fig.2 BLOCK DIAGRAM

◇PIN CONFIGURATION

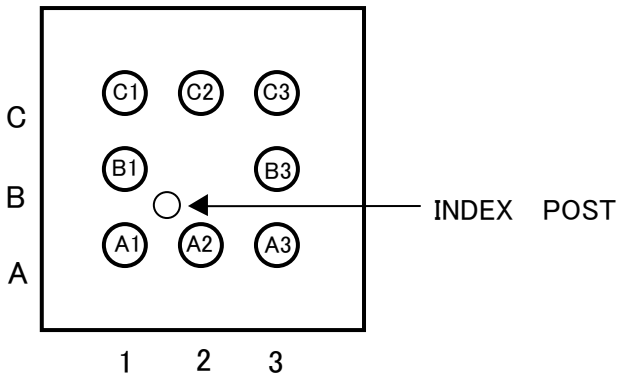

Fig-3 BU9832GUL-W (bottom view)

◇PIN NAME

Land No.	PIN NAME	I/O	FUNCTION
A1	$\overline{WP}$	IN	Write Protect Input When WPEN bit is high in status register, $\overline{WP}$ input pin become active and is able to inhibit "Write Status Register"
A2	GND	—	Ground (0V)
A3	SI	IN	Start Bit, Op.code, Address, Serial Data Input
B1	SO	OUT	Serial Data Output
B3	SCK	IN	Serial Data Clock Input
C1	$\overline{CS}$	IN	Chip Select Control
C2	Vcc	—	Power Supply
C3	$\overline{HOLD}$	IN	Hold Input Hold Input is able to suspend data transmission for a time.

◇SYNCHRONOUS DATA TIMING

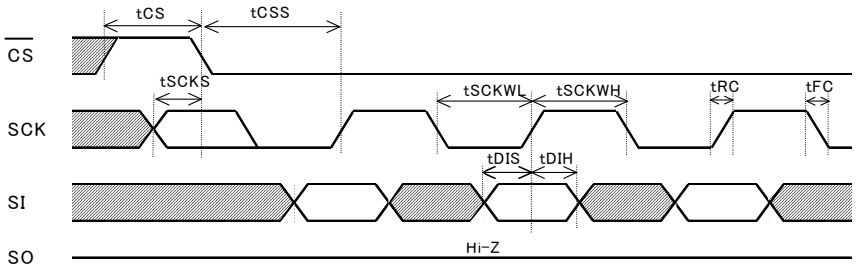

Fig.4 DATA INPUT TIMING

SI data is latched into the chip at the rising edge of SCK clock.
Address and data must be transferred from MSB.

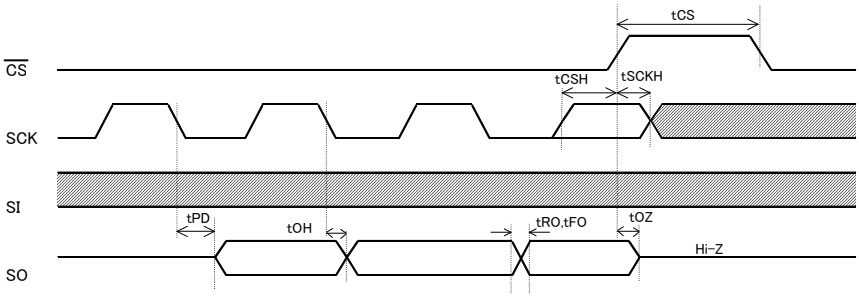

Fig.5 INPUT AND OUTPUT TIMING

SO data toggles at the falling edge of SCK clock.
Output data toggles from MSB.

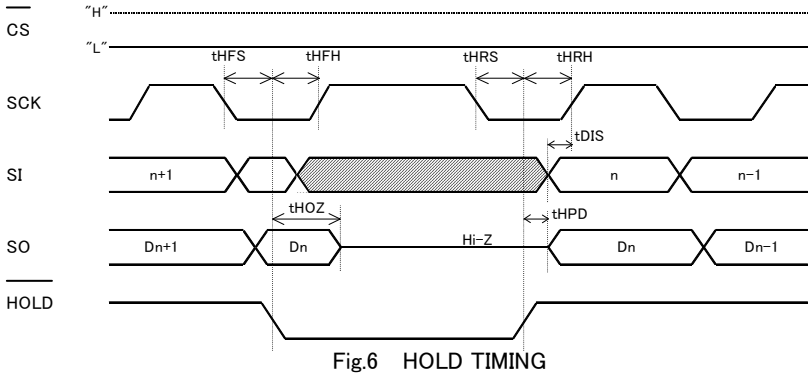

Fig.6 HOLD TIMING

AC Condition

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Load Capacitance 1	CL1	–	–	100	pF
Load Capacitance 2	CL2	–	–	30	pF
Input Rise times	–	–	–	50	ns
Input Fall times	–	–	–	50	ns
Input Pulse Voltage	–	0.2Vcc/0.8Vcc			V
Input and Output Timing Reference Voltages	–	0.3Vcc/0.7Vcc			V

◇AC OPERATING CHARACTERISTICS (Ta=-40～85℃)　　*Load capacitance1 C_{L1}=100pF

Parameter	Symbol	1.8≦Vcc＜2.5V			2.5≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK clock Frequency	fSCK	–	–	2	–	–	5	MHz
SCK High Time	tSCKWH	200	–	–	85	–	–	ns
SCK Low Time	tSCKWL	200	–	–	85	–	–	ns
$\overline{CS}$ High Time	tCS	200	–	–	85	–	–	ns
$\overline{CS}$ Setup Time	tCSS	200	–	–	90	–	–	ns
$\overline{CS}$ Hold Time	tCSH	200	–	–	85	–	–	ns
SCK Setup Time	tSCKS	200	–	–	90	–	–	ns
SCK Hold Time	tSCKH	200	–	–	90	–	–	ns
SI Setup Time	tDIS	40	–	–	20	–	–	ns
SI Hold Time	tDIH	50	–	–	40	–	–	ns
Output Data Delay Time1	tPD1	–	–	150	–	–	70	ns
Output Data Delay Time2 (CL2=30pF)	tPD2	–	–	145	–	–	55	ns
Output Hold Time	tOH	0	–	–	0	–	–	ns
Output Disable Time	tOZ	–	–	250	–	–	100	ns
Clock High Setup Time before $\overline{HOLD}$ Active.	tHFS	120	–	–	60	–	–	ns
Clock Low Hold Time after $\overline{HOLD}$ Active.	tHFH	90	–	–	40	–	–	ns
Clock High Setup Time before $\overline{HOLD}$ not Active.	tHRS	120	–	–	60	–	–	ns
Clock Low Hold Time after $\overline{HOLD}$ not Active.	tHRH	140	–	–	70	–	–	ns
$\overline{HOLD}$ to Output High-Z	tHOZ	–	–	250	–	–	100	ns
$\overline{HOLD}$ to Output Valid	tHPD	–	–	150	–	–	70	ns
SCK Rise Time *1	tRC	–	–	1	–	–	1	μs
SCK Fall Time *1	tFC	–	–	1	–	–	1	μs
Output Rise Time *1	tRO	–	–	100	–	–	50	ns
Output Fall Time *1	tFO	–	–	100	–	–	50	ns
Write Cycle Time	tE/W	–	–	5	–	–	5	ms

*1 Not 100% TESTED

◇Functional Description

○Status Register

The device has status register.
Status register consists of 8bits and is shown following parameters.
3bits(WPEN, BP0 and BP1) are set by "Write Status Register" commands, which are non-volatile.
Specification of endurance and data retention are as well as memory array.
WEN bit is set by "Write enable" and "Write Disable" commands. After power become on, the device is disable mode. $\overline{R}$/B bit is a read-only and status bit. The device is clocked out value of the status register by "Read Status Register" command input.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

×:Don't care

Bit	Definition
WPEN	$\overline{WP}$ pin ENABLE Bit WPEN=0 : no use WPEN=1 Protect
BP0/BP1	Block write protection for memory array (EEPROM)
WEN	Write enable/disable state bit WEN=0 : write disable WEN=1 : write enable
$\overline{R}$/B	READY／BUSY status bit $\overline{R}$/B=0 : READY $\overline{R}$/B=1 : BUSY

Table1. Status Register

BP1	BP0	Block Write Protection
0	0	None
0	1	300h-3FFh
1	0	200h-3FFh
1	1	000h-3FFh

Table2. Block Write Protection

○$\overline{WP}$ pin

The device inhibits to write the data into status register during $\overline{WP}$ is low. WPEN bit in status register needs to be high to enable $\overline{WP}$ pin function.

○$\overline{HOLD}$ pin

$\overline{HOLD}$ pin is able to suspend data transmission for a time (Hold state). $\overline{HOLD}$ pin is normally high for transmission of the data. SCK and SI input are "Don't Care" and SO output state is Hi-Z for hold state.
After $\overline{HOLD}$ pin is brought high to release hold state during SCK is low, the device resumes to transfer the data. For example, in case the device is hold state after A5 (the address data) input in read command, to resume the data transmission enable starting A4 (the address data) input after hold state is release. When $\overline{CS}$ is brought high with hold state, the device is reset and cannot resume the data transmission.

◇INSTRUCTION CODE

Instruction	Operation	Op.Code	Address
WREN	Write enable	0000 0110	—
WRDI	Write disable	0000 0100	—
READ	Read data from memory array	0000 0011	A9 ～ A0
WRITE	Write data to memory array	0000 0010	A9 ～ A0
RDSR	Read status register	0000 0101	—
WRSR	Write status register	0000 0001	—

◇TIMING CHART

1.WREN (WRITE ENABLE)

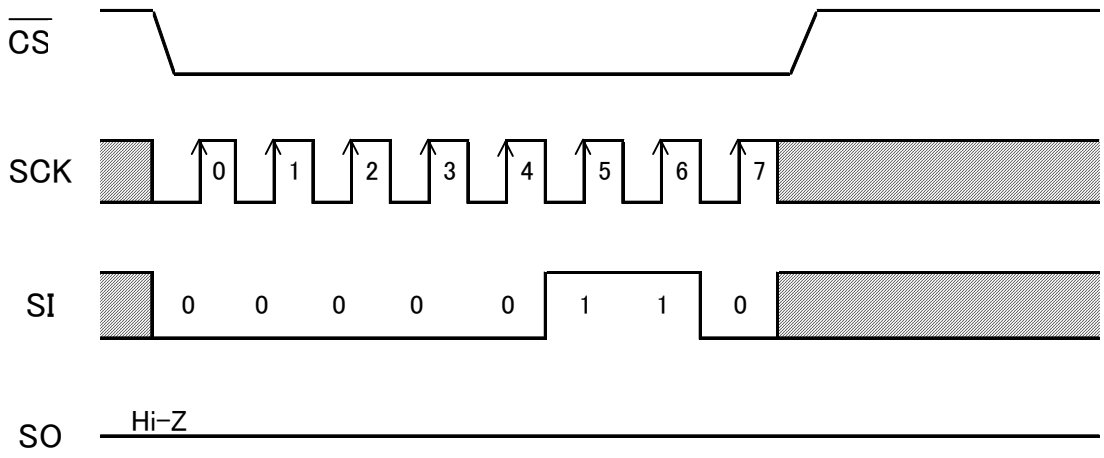

Fig.7 WRITE ENABLE CYCLE TIMING

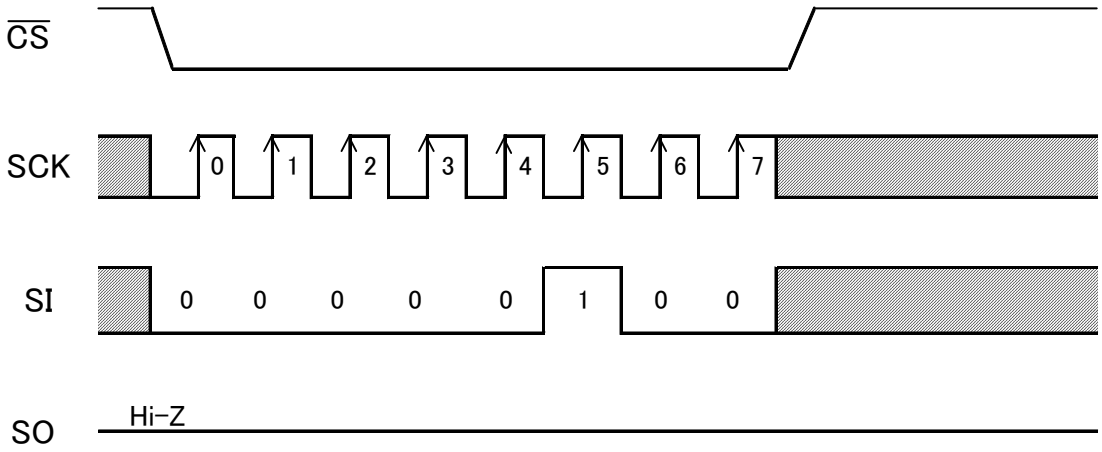

Fig.8 WRITE DISABLE CYCLE TIMING

2.WRDI (WRITE DISABLE)

The device has both of the enable and disable mode. After "Write Enable" is executed, the device becomes in the enable mode. After "Write Disable" is executed, the device becomes in the disable mode. After $\overline{CS}$ goes low, each of Op.code is recognized at the rising edge of 7th clock. Each of instructions is effective inputting seven or more SCK clocks.

This "Write Enable" instruction must be proceeded before the any write commands.

The device ignores inputting the any write commands in the disable mode.

Once the any write commands is executed in the enable mode, the device becomes the disable mode.

After the power become on, the device is in the disable mode.

3.READ

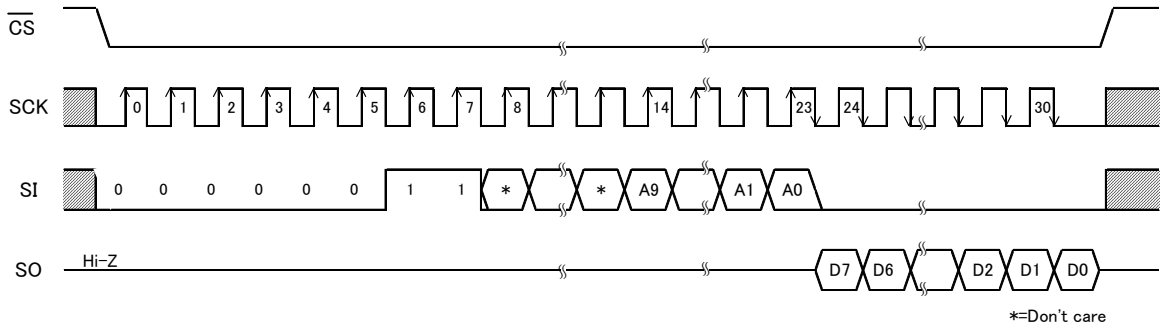

Fig.9 READ CYCLE TIMING

The data stored in the memory are clocked out after "Read" instruction is received.
After $\overline{CS}$ goes low, the address need to be sent following by Op.code of "Read".
The data at the address specified are clocked out from D7 to D0, which is start at the falling edge of 23th clock.
This device has the auto-increment feature that provides the whole data of the memory array with one read command, outputs the next address data following the addressed 8bits of data by keeping SCK clocking. When the highest address is reached, the address counter rolls over to the lowest address allowing the continuous read cycle.

4.WRITE

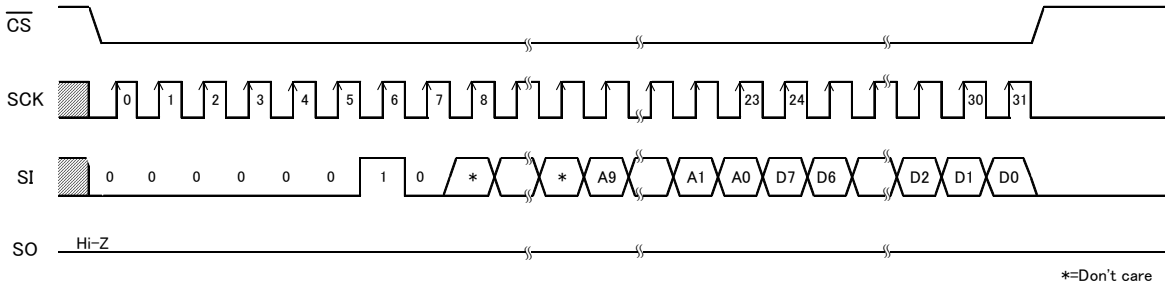

Fig.10 WRITE CYCLE TIMING

This "Write" command writes 8bits of data into the specified address. After $\overline{CS}$ goes low,the address need to be sent following by Op.code of "Write". Between the rising edge of the 31th clock and it of the 32th clock, the rising edge of $\overline{CS}$ initiates high voltage cycle, which writes the data into non-volatile memory array, but the command is cancelled if $\overline{CS}$ is high except that period. It takes maximum 5ms in high voltage cycle (tE/W). The device does not receive any command except for "Read Status Register" command during this high voltage cycle.

This device is capable of writing the data of maximum 32byte into memory array at the same time, which keep inputting two or more byte data with $\overline{CS}$ "L"after 8bits of data input.

For this Page Write commands, the six higher order bits of address are set, the four low order address bits are internally incremented by 5bits of data input.

If more than 32 words, are transmitted the address counter "roll over", and the previous transmitted data is overwritten.

5. RDSR (READ STATUS REGISTER)

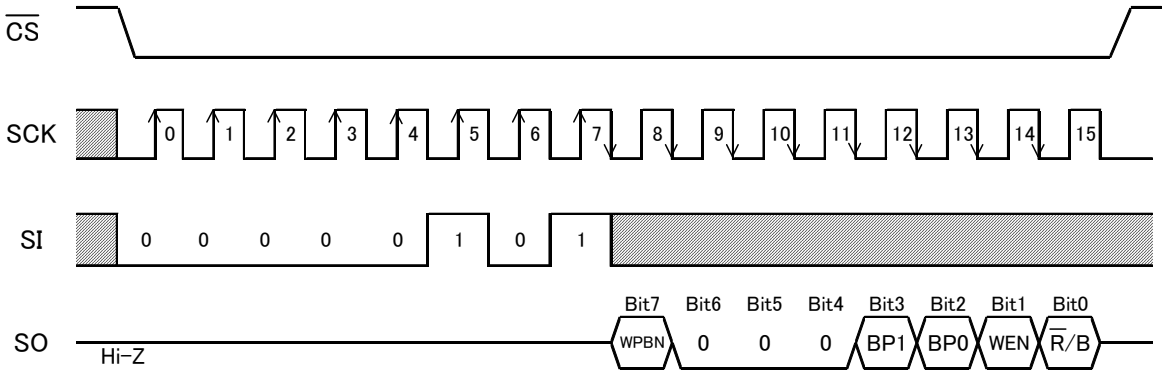

Fig.11 READ STATUS REGISTER CYCLE TIMING

The data stored in the status register is clocked out after "Read Status Register" instruction is received.
After $\overline{CS}$ goes low, Op.code of "Read Status Register" need to sent.
The data stored in the status register is clocked out of the device on the falling edge of 7th clock. Bit6, Bit5 and Bit4 in the status register are read as 0.
This device has the auto-increment feature as well as "Read" that outputs the 8bits of the same data following it to keep SCK clocking.
It is possible to see ready and busy state by executing this command during tE/W.

5.WRSR (WRITE STATUS RESISTER)

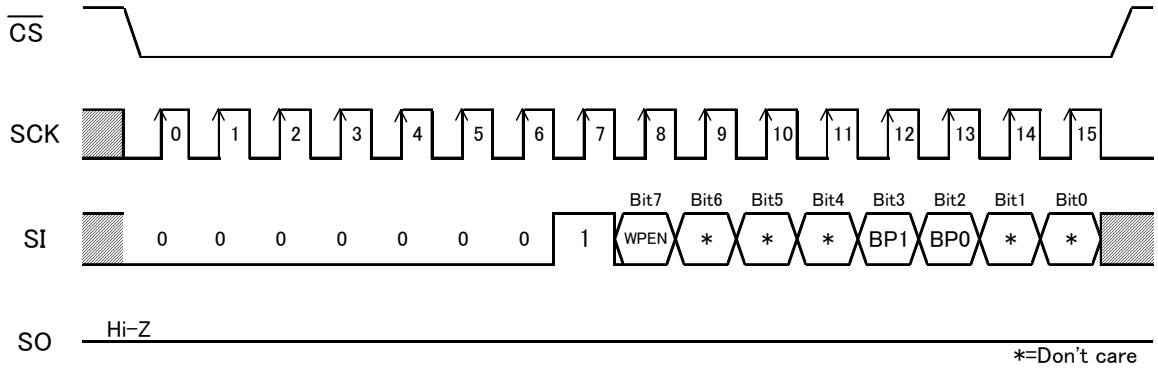

Fig.12 WRITE STATUS REGISTER WRITE CYCLE TIMING

This "Write Status Register" command writes the data, two (BP1, BP0) of the eight bits, into the status register. Write protection is set by BP1 and BP0 bits.

After $\overline{CS}$ goes low, Op.code of "Read Status Register" need to sent. Between the rising edgeof the 15th clock and it of the 16th clock, the rising edge of $\overline{CS}$ initiates high voltage cycle, which writes the data into non-volatile memory array, but the command is cancelled if $\overline{CS}$ is high exceptthat period. It takes maximum 5ms in high voltage cycle (tE/W) as well as "Write".Block write protection is determined by BP1 and BP0 bits, which is selected from quarter, half and the entire memory array. (See Table2 BLOCK WRITE PROTECTION.)

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