Structure Silicon Monolithic Integrated Circuit

Product Name LED Driver for cellular phone

Type **BD82103GWL**

Features
- 2light or 3light parallel LED driver is mounted
- 16-step LED current adjust function
- Inter-LED relative current accuracy: 5% or less
- Driving control via a single-line digital control interface
- Automatic transition charge pump type DC/DC converter (×1,×1.5, ×2)
- High efficiency achieved (90% or more at maximum)
- It transits for the most suitable power operating by the LED terminal process of the 3rd light when 2 light driving
- Various protection functions such as output voltage protection and thermal shutdown circuit are mounted.
- Package : UCSP50L1 (Thick 0.55mm MAX, Pin pitch 0.4mm) CSP11pin package

○Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	VMAX	7	V
Power dissipation	Pd	730	mW
Operating temperature range	Topr	-30 ~ +85	°C
Storage temperature range	Tstg	-55 ~ +150	°C

Note 1) The measurement value which was mounted on the PCB by ROHM.
When a glass epoxy substrate (70mm x 70mm x 1.6mm) has been mounted, this loss will decrease 5.84mW/°C if Ta is higher than or equal to 25°C.

○Operating Conditions (Ta = -30 ~ 85 °C)

Parameter	Symbol	Limits	Unit
Operating power supply voltage	VBAT	2.7 ~ 5.5	V

*This chip is not designed to protect itself against radioactive rays.

○Electrical Characteristics (Unless otherwise noted, Ta = +25°C, VBAT=3.6V)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Input voltage range	V_{in}	2.7	3.6	5.5	V	VBAT terminal
Quiescent Current	I_q	-	0.1	1	μA	EN=0V
Current Consumption1	I_{dd1}	-	1.0	2.4	mA	×1.0 Mode, Except LED current
Current Consumption2	I_{dd2}	-	2.0	3.5	mA	×2.0 Mode, Except LED current
Charge Pump						
Oscillator frequency	f_{OSC}	0.56	0.85	1.14	MHz	
Current Source						
LED maximum current	$I_{LED-max}$	18	20	22	mA	VBAT≥3.0V
LED current accuracy	$I_{LED-diff}$	-	-	10.0	%	When LED current 10.0mA setting and LED terminal voltage 1.0V
LED current matching	$I_{LED-match}$	-	0.5	5.0	%	When LED current 10.0mA setting and LED terminal voltage 1.0V
LED control voltage	V_{LED}	-	0.15	0.25	V	Minimum voltage at LED1~LED3 pins
Logic control terminal						
Low threshold voltage	V_{IL}	-	-	0.4	V	EN
High threshold voltage	V_{IH}	1.4	-	-	V	EN
High level Input current	I_{IH}	-	0	1	μA	EN=Vin
Low level Input current	I_{IL}	-1	0	-	μA	EN=0V
Minimum EN High time	T_{HI}	0.05	-	100	μsec	Described in Fig.1
Minimum EN Low time	T_{LO}	0.3	-	100	μsec	Described in Fig.1
EN Off Timeout	T_{OFF}	1	-	-	msec	Described in Fig.1
Latch time	T_{LAT}	1	-	-	msec	Described in Fig.1
Access available time	T_{acc}	1	-	-	msec	Described in Fig.1

▪ Register access control protocol

LED current is controlled by only EN terminal. It is possible to access the register inside of this chip by using the protocol below. LED driver ON/OFF, selecting the mode is operated by accessing the registers with using this protocol.

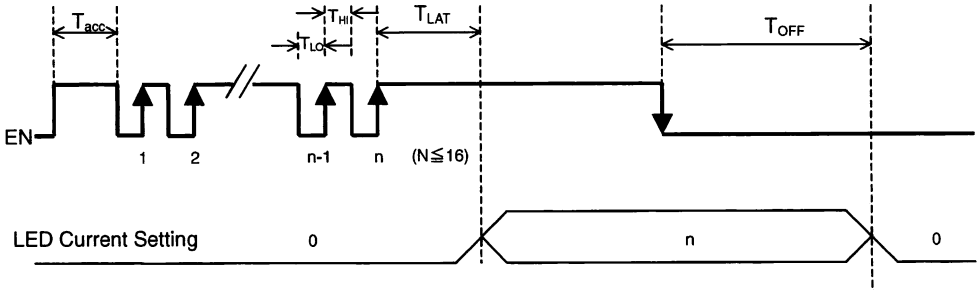
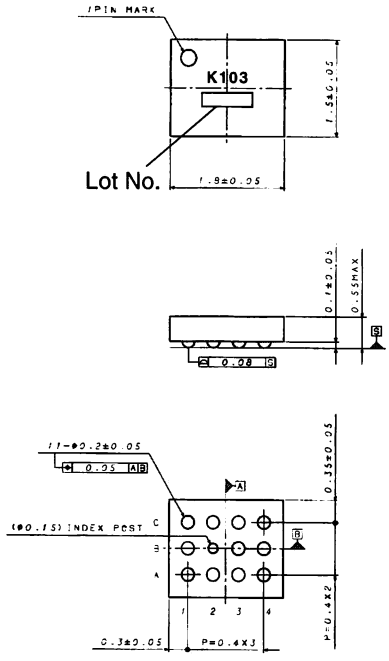


Fig.1 Register access protocol

(Note) ▪ In the case of N > 16, BD82103GWL selects the mode of N = 16.
▪ Refresh the registers periodically.
▪ Reset BD82103GWL of the time of set unusual operation.

○Package Outline



VCSP50L1 (11pin)　(Unit : mm)

○Pin Description

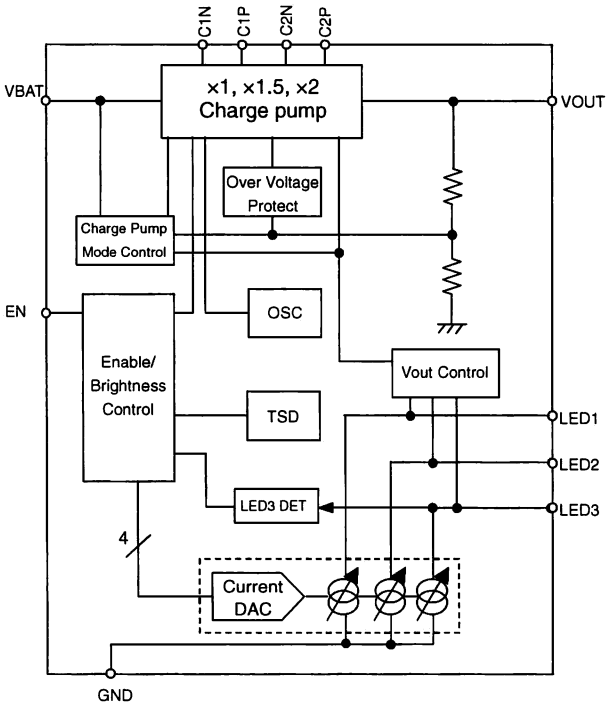
PIN No.	PIN Name
C3	VBAT
B4	C1P
C4	C1N
A4	C2P
A3	C2N
A2	VOUT
B3	EN
C1	LED1
B1	LED2
A1	LED3
C2	GND

○LED current level

Data	Output current [mA]	Data	Output current [mA]
1	20.0	9	5.0
2	17.0	10	4.0
3	14.0	11	3.0
4	12.0	12	2.0
5	10.0	13	1.0
6	8.5	14	0.5
7	7.0	15	0.25
8	6.0	16	0.125

Please refer to an attached sheet "BD82103GWL Function Description" about a detailed function.

○Block diagram



Pin number　11pin

Fig. 2 Block Diagram

○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line

Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage

Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

(4) Short circuit between pins and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) LDO

Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that an operation becomes unstable.

(11) About the pin for the test, the un-use pin

Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(12) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

(13) About the function description or application note or more.

The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements.

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