

Structure Silicon Monolithic Integrated Circuit
 Product name Digital input D class headphone amplifier for mobile phone

Type **BU7839GVW**

- Feature
- BU7839GVW have Stereo Audio DAC and HPamp function
 - Low power consumption and high efficiency for digital audio player
 - Anti pop sound and muting transistor included
 - Lch, Rch independent digital gain control volume
 (Immediately change, zero cross change, soft change)
 - Sampling frequency 8kHz~48kHz
 - PLL included (master mode / slave mode)
 - Soft mute function included
 - 2wire CPU I/F (two address selection 33h or 36h)

○Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Analog Supply Voltage	AVDD	-0.3 ~ 4.5	V
Digital Supply Voltage	DVDD	-0.3 ~ 2.1	V
Digital I/O Supply Voltage	DVDDIO	-0.3 ~ 4.5	V
Terminal applied voltage 1	VIN1	DVSS-0.3 ~ DVDDIO+0.3	V
Terminal applied voltage 2 *1	VIN2	DVSS-0.3 ~ 4.5	V
Power Dissipation	Pd	520 *2	mW
Storage Temperature Range	Tstg	-50 ~ 125	°C
Operation Temperature Range	Topr	-30 ~ 85	°C

*1 Terminal SCL and SDA

*2 This is the power dissipation per IC unit. Reduce to 52 mW/°C when Ta = 25°C or above.
 When 114.6mm x 76.2mm x 1.6mm is mounted

○Operating condition (Unless otherwise noted, Ta = 25°C).

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Analog Supply Voltage	AVDD	2.5	2.8	3.0	V
Digital I/O Supply Voltage	DVDDIO	DVDD	-	3.0	V
Digital Supply Voltage	DVDD	1.35	1.50	1.65	V

This chip is not designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Electrical characteristics

Ta=25°C, DVDD=DVDDIO=1.5V, VDD_R=VDD_L=PLLVD=2.8V, REFCLK=12MHz, fs=44.1kHz, f=1kHz, Load=16Ω, A-weight, 20kHz LPF, Slave mode

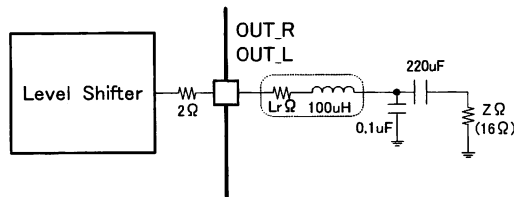
Parameter	Symbol	Limit			Unit	Note
		MIN	TYP	MAX		
Standby current DVDD	IDDst	-	-	10	uA	Stand-by
Standby current VDD_R+VDD_L	ICCst	-	-	10	uA	Stand-by
Standby current PLLVD	IPLLst	-	-	10	uA	Stand-by
Current consumption DVDD	IDD	-	0.6	2.0	mA	When 0.1mW is output (At slave mode)
Current consumption VDD_R+VDD_L	ICC	-	2.0	6.0	mA	When 0.1mW is output
Current consumption PLL	IPLL	-	0.8	2.5	mA	
Output level gain error	Vout	-2	-	2	dB	The difference and it the following refers to the reference when 0dBFS is output.
Channel gain error	Gerr	-1	-	1	dB	Lch-Rch
S/N	SN	60	80	-	dB	0dBFS, A-Weight
THD+N	THD	-40	-60	-	dB	-3dBFS, A-Weight
Channel isolation	ISO	65	80	-	dB	0dBFS, 1kHz BPF
PSRR	PSRR	-	0	-	dB	

※Output level gain error

Equivalent series resistance of coil reduces output level.

Equivalent series resistance = $L_r[\Omega]$, $VDD_R = VDD[V]$, $VDD_L = VDD[V]$, Output load impedance = $Z[\Omega]$

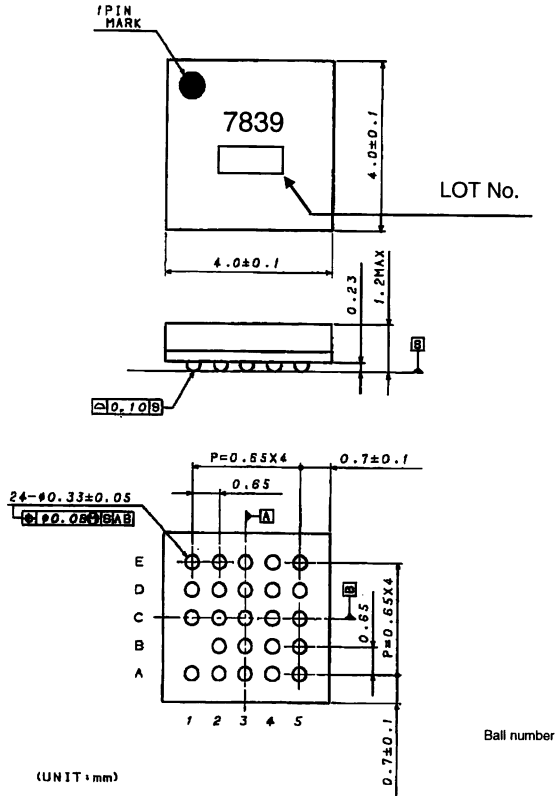
$$\text{Output Reference Level [Vpp]} = VDD \times 0.5 \times Z / (L_r + Z + 2)$$



For example output reference level and output power, when equivalent series resistance is 0.0Ω, 0.7Ω, 4Ω, 7Ω and VDD=2.8V, output load impedance=16Ω

Equivalent Series Resistance [Ω]	Output Reference Level [Vpp]	Output Reference Level [dBV]	Output Power [mW]
0.0	1.24	-7.13	12.10
0.7	1.20	-7.46	11.21
4.0	1.02	-8.87	8.10
7.0	0.90	-9.98	6.27

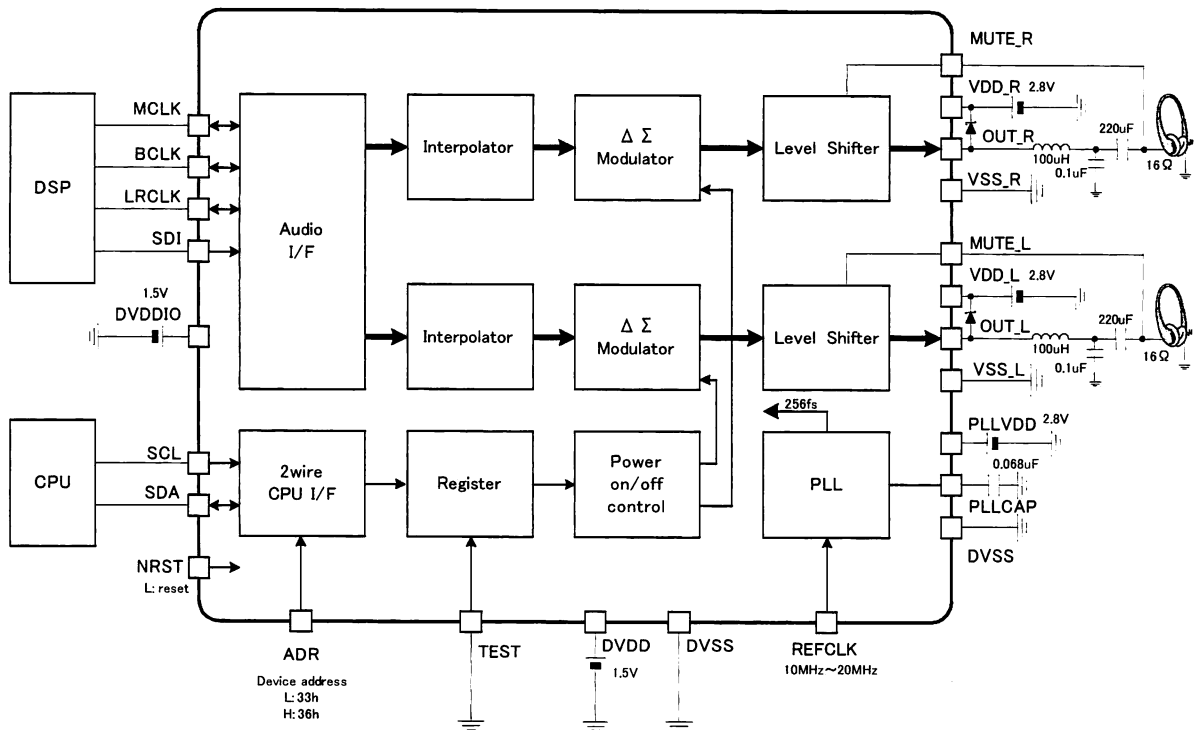
External measure and View



Pin assignment

No	Pin name	Function
A1	MCLK	Audio I/F Master clock
B3	BCLK	Audio I/F Bit clock
A2	LRCLK	Audio I/F LR clock
C2	SDI	Audio I/F Serial data
C1	DVDDIO	Digital IO VDD
B4	SCL	2wire CPU I/F serial clock
A5	SDA	2wire CPU I/F serial data
B2	NRST	Reset
A3	ADR	Device address select
C3	TEST	Test pin
D1	DVDD	Digital core VDD
A4	DVSS	Digital core VSS
B5	REFCLK	Reference clock
D5	PLLVDD	PLL VDD
C5	PLLCAP	PLL capacitor
C4	DVSS	PLL, Digital VSS
D4	VDD_R	Analog VDD
E4	OUT_R	Rch output
E5	MUTE_R	Rch mute
D3	VSS_R	Analog VSS
E1	VDD_L	Analog VDD
E2	OUT_L	Lch output
D2	MUTE_L	Lch mute
E3	VSS_L	Analog VSS

Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

(13) Others

In case of use this LSI, please peruse some other detail documents, we called Application note.

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