Middle Power Class-D Speaker Amplifiers

Analog Input / BTL Output Class-D Speaker Amplifier

BD5413EFV

No.10075EBT01

●Description

BD5413EFV is a 5W + 5W stereo class-D power amplifier specifically developed for low power consumption and low heat generation applications like powered speakers. BD5413EFV employs the state-of-the-art BCD (Bipolar, CMOS and DMOS) process technology to eliminate a turn-on resistance in the output power stage and an internal loss due to a wiring resistance as much as possible, achieving a high performance of 80% (4W + 4W output with a load resistance of 8Ω). In addition, BD5413EFV employs a compact power package which dissipates heat via the rear to achieve low power consumption and low heat generation so that the need for connecting an external heat radiator can be eliminated up to a total output of 12.8W. This product meets the needs for compact, thin sound generation systems and powerful, high-quality sound reproduction.

●Features

1) Small output noise voltage capable of achieving a high S/N set
   Input conversion noise voltage = 2.8μVrms
   A bipolar differential is used for input amplifier to eliminate 1/f noise.
2) Support of power supply voltage ranging from 6V to 10.5V
   A supply voltage range is supported that matches an AC adaptor or battery cell driven set.
   When a set is battery driven, its operating time can be extended by means of a high performance class-D amplifier.
3) Support of low current consumption mode
   A circuit current in shut-down mode is 1μA or less.
4) Built-in soft muting function for reducing pop at shut-down ON or OFF
   When a signal is present, its smooth envelope waveform is realized owing to this function.
   In addition, when no signal is present, pop generation is eliminated.
   A transit time can be adjusted easily through the use of an external capacitor.
5) Realization of high efficiency and low heat generation
   Efficiency = 80% (4W+4W (Vcc=9V, R_L=8Ω) output can be made without using an external heat radiator.)
   A compact power package HTSSOP-B24 (7.8mm x 7.6mm) is employed.
6) Built-in function for reducing pop generation at disconnection from the outlet
7) Support of function for sampling frequency selection
   An internal PWM sampling frequency can be selected from three frequencies (200kHz, 250kHz and 300kHz).
   Countermeasures against interference (beat noise) due to a switching power source can be taken as needed.
8) Realization of high reliability
   Countermeasures against short-circuits due to output terminals shorted to V_{CC} or ground can be taken (support of automatic recovery).
   A temperature protection circuit is incorporated (support of automatic recovery).
9) Support of ERROR pin
   ERROR output takes place as a warning which indicates an error.
   (short-circuits due to output terminals shorted to V_{CC} or ground, or IC high temperature abnormality).

●Absolute maximum ratings

A circuit must be designed and evaluated not to exceed absolute maximum rating in any cases and even momentarily, to prevent reduction in functional performances and thermal destruction of a semiconductor product and secure useful life and reliability.

The following values assume Ta =25℃. For latest values, refer to delivery specifications.

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	+15	V	Pin 3, 5, 10, 12, 16, 21 (Note 1,2)
Power dissipation	P_d	1.1	W	(Note 3)
		2.8	W	(Note 4)
Input voltage for signal pin	V_{IN}	-0.2 to Vcc+0.2	V	Pin 23, 24 (Note 1)
Input voltage for control pin	V_{CONT}	-0.2 to Vcc+0.2	V	Pin 14, 15 (Note 1)
Operating temperature range	Topr	-40 to +85	℃	
Storage temperature range	Tstg	-55 to +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

(Note 1) A voltage that can be applied with reference to GND (pins 1, 7, 8, 13, 18 and 19)
(Note 2) Pd and Tjmax=150℃ must not be exceeded.
(Note 3) 70mm × 70mm × 1.6mm FR4 One-sided glass epoxy board (Back copper foil 0%) installed.
If used under Ta=25℃ or higher, reduce 8.8 mW for increase of every 1℃. The board is provided with thermal via.
(Note 4) 70mm × 70mm × 1.6mm FR4 Both-sided glass epoxy board (Back copper foil 100%) installed.
If used under Ta=25℃ or higher, reduce 22.4 mW for increase of every 1℃. The board is provided with thermal via.

●Operating conditions

The temperature (Ta) is 25℃. For the latest temperature, refer to the delivery specifications.

Parameter	Symbol	Ratings	Unit	Conditions
Supply voltage	VCC	+6 to +10.5	V	Pin 3, 5, 10, 12, 16, 21
Load resistance	R_L	6 to 16	Ω	(Note 5)

(Note 5) This value must not exceed Pd.

●Electrical characteristics

Unless otherwise stated, Ta=25℃, Vcc=9V, f_{IN}=1kHz, Rg=0Ω, RL=8Ω, SDX="H" and FC="M (OPEN)" are assumed. For the latest values, refer to the delivery specifications.

Parameter	Symbol	Limits	Unit	Conditions
Whole circuit				
Circuit current 1 (sampling mode)	I_{CC1}	12	mA	No signal, no load
Circuit current 2 (mute mode)	I_{CC2}	1	μA	SDX = “L”
Control				
Input voltage with SDX pin set to "H"	V_{IHSDX}	2.5 to 9	V	Sampling state
Input voltage with SDX pin set to "L"	V_{ILSDX}	0 to 0.5	V	Shut-down state
Input voltage with FC pin set to "H"	V_{IHFC}	8.2 to 9	V	Setting of Fs=300kHz
Input voltage with FC pin set to "M"	V_{IMFC}	3.8 to 5.2	V	Setting of Fs=250kHz
Input voltage with FC pin set to "L"	V_{ILFC}	0 to 0.8	V	Setting of Fs=200kHz
Audio output				
Voltage gain	G_V	30	dB	P_O = 1W
Maximum output power 1 (Note 6)	P_{O1}	4	W	THD+N = 10%, RL = 8Ω
Maximum output power 2 (Note 6)	P_{O2}	5	W	THD+N = 10%, RL = 6Ω
Total harmonic distortion ratio (Note 6)	THD	0.2	%	P_O = 1W, BW=20Hz to 20kHz
Crosstalk	CT	65	dB	P_O = 1W, Rg = 0Ω, BW = IHF-A
Output noise voltage (sampling mode)	V_{NO}	90	μVrms	Rg = 0Ω, BW = IHF-A
Residual noise voltage (mute mode)	V_{NOM}	1	μVrms	Rg = 0Ω, BW = IHF-A, MUTEX = “L”
Internal sampling clock frequency	F_S	200	kHz	FC = L
		250		FC = M(OPEN)
		300		FC = H

(Note 6) The rated values of items above indicate average performances of the device, which largely depend on circuit layouts, components, and power supplies. The reference values are those applicable to the device and components directly installed on a board specified by us.

●Electrical characteristic curves (Ta=25℃) (Reference data)

(1) Under Stereo Operation (R_L=8Ω)

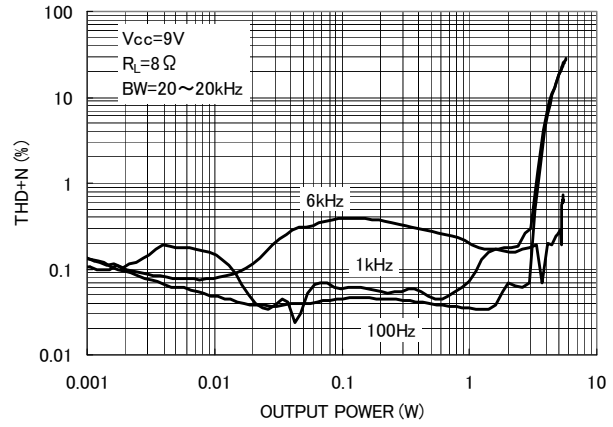


Fig. 1 THD+N - Output Power

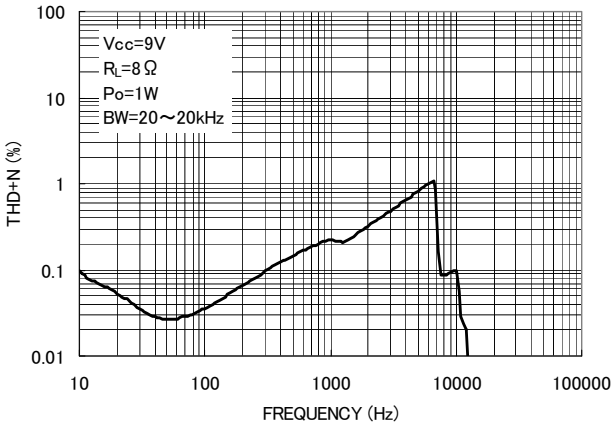


Fig. 2 THD+N - Frequency

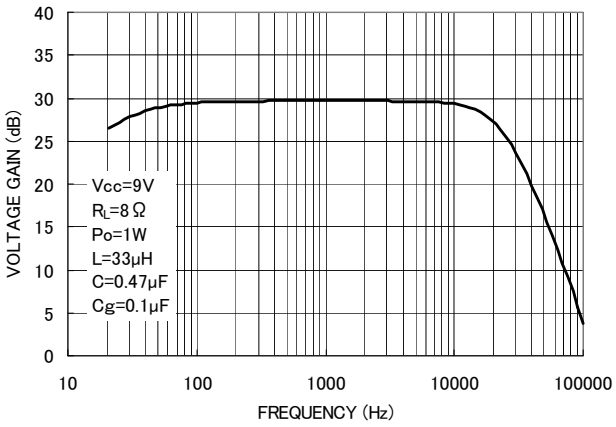


Fig. 3 Voltage Gain - Frequency

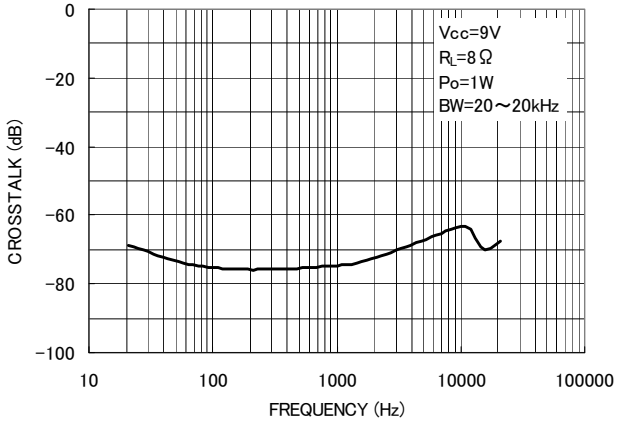


Fig. 4 Crosstalk - Frequency

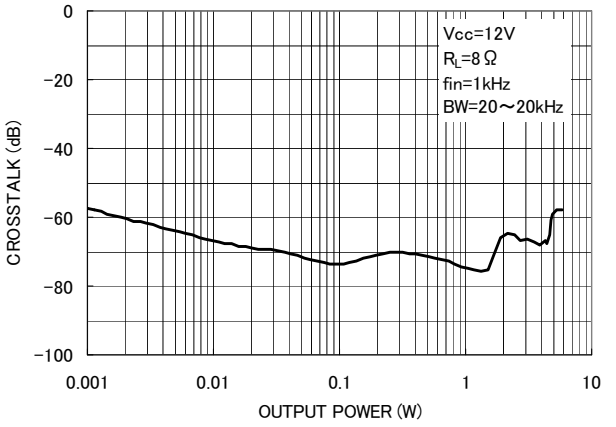


Fig. 5 Crosstalk - Output Power

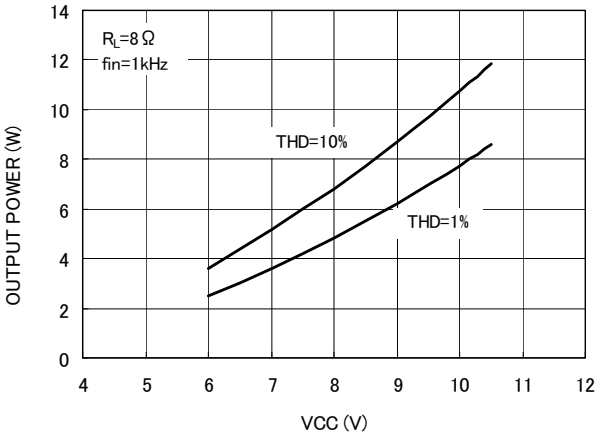


Fig. 6 Output Power - Supply Voltage

●Electrical characteristic curves (Reference data) – Continued

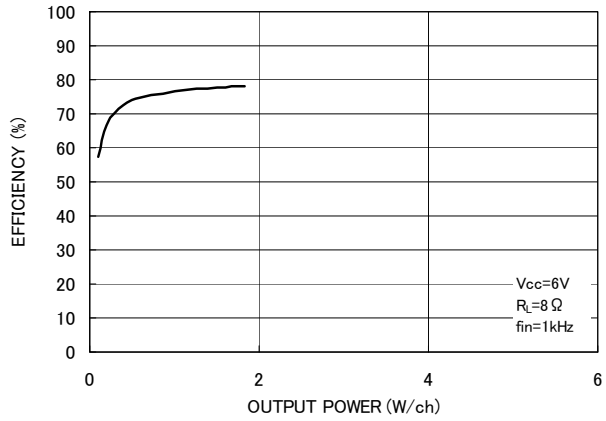


Fig. 7 Efficiency - Output Power

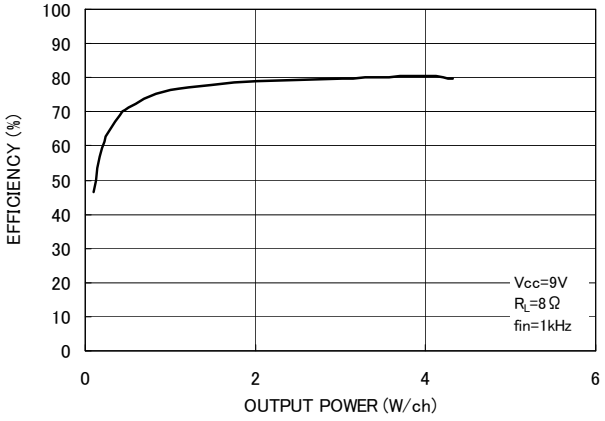


Fig. 8 Efficiency - Output Power

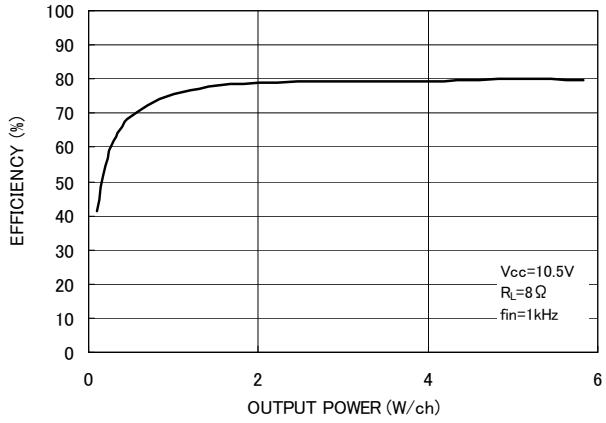


Fig. 9 Efficiency - Output Power

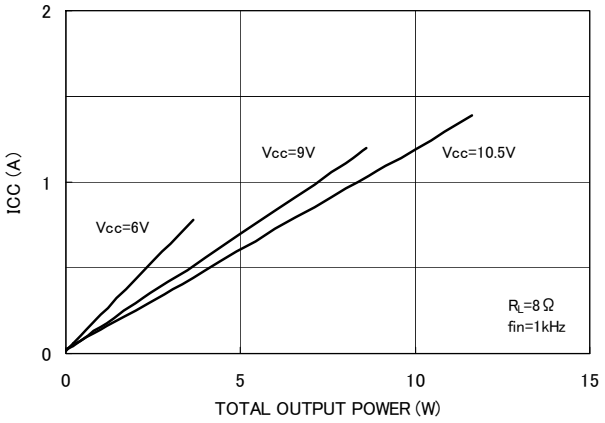


Fig. 10 Current Consumption - Output Power

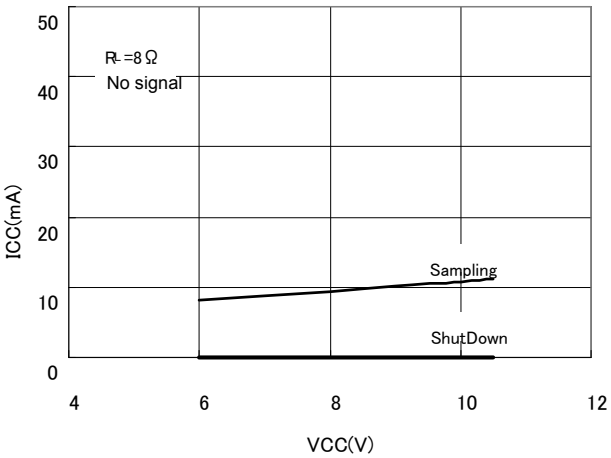


Fig. 11 50 Current Consumption - Supply Voltage

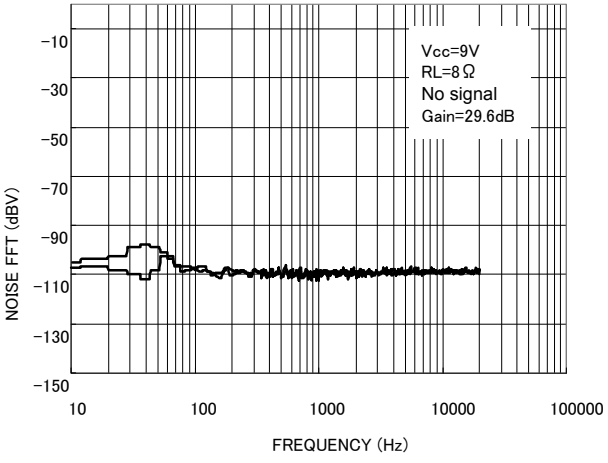


Fig. 12 Output Noise Voltage FFT

●Electrical characteristic curves (Reference data) – Continued

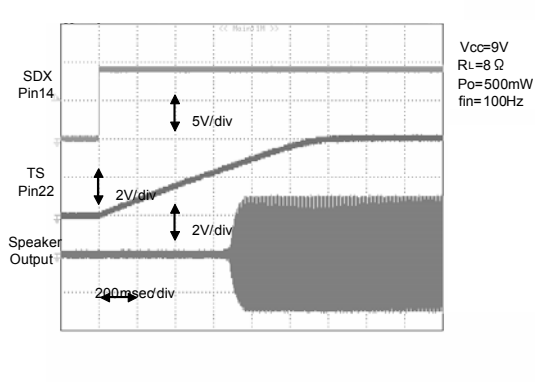


Fig. 13 Waveform at Soft Mute Reset

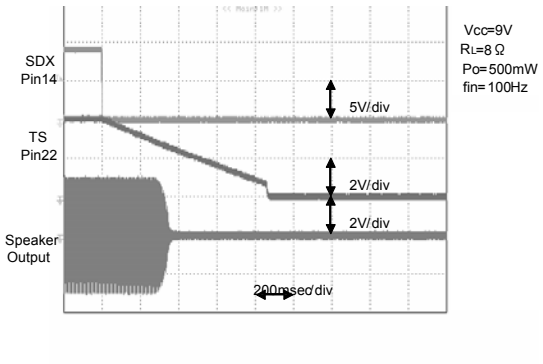


Fig. 14 Waveform at Soft Mute

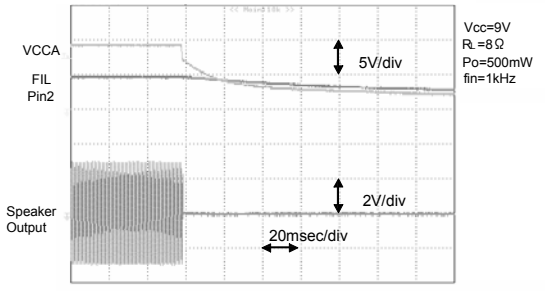


Fig. 15 Waveform at Instantaneous Power Interruption (20msec/div)

●Electrical characteristic curves (Reference data) – Continued

(2) Under Stereo Operation (R_L=16 Ω)

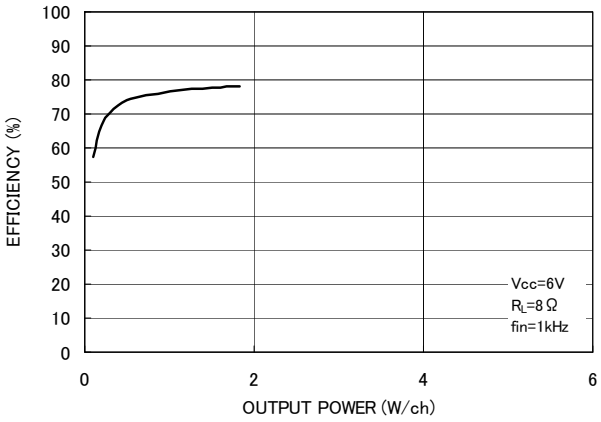


Fig. 16 Output Power - Supply Voltage

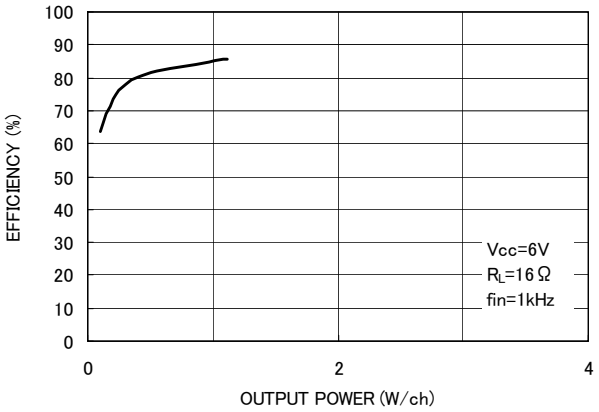


Fig. 17 Efficiency - Output Power

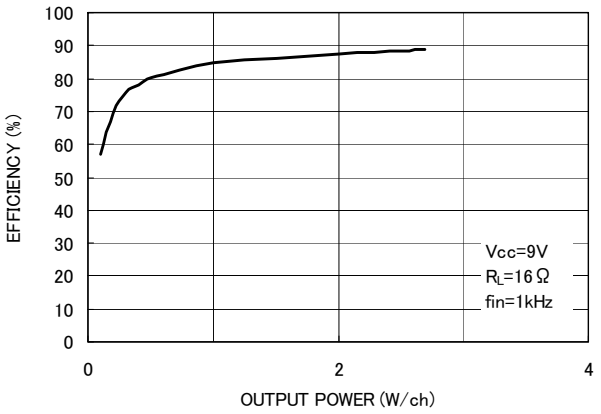


Fig. 18 Efficiency - Output Power

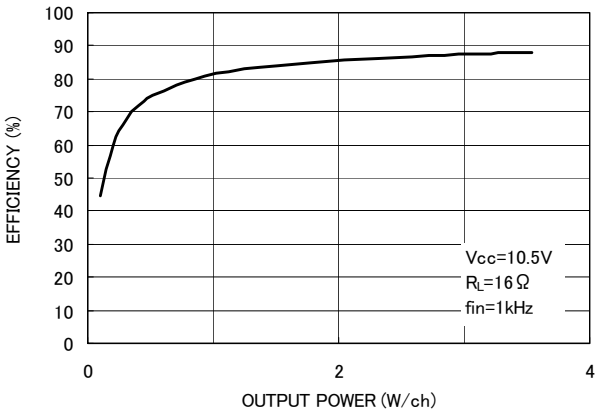


Fig. 19 Efficiency - Output Power

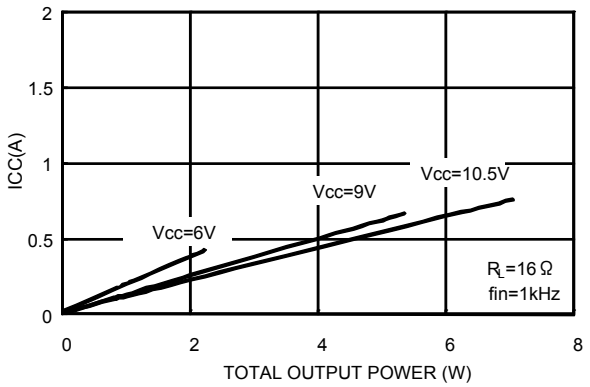


Fig. 20 Current Consumption - Output Power

●Electrical characteristic curves (Reference data) – Continued

(3) Under Stereo Operation (R_L=6Ω)

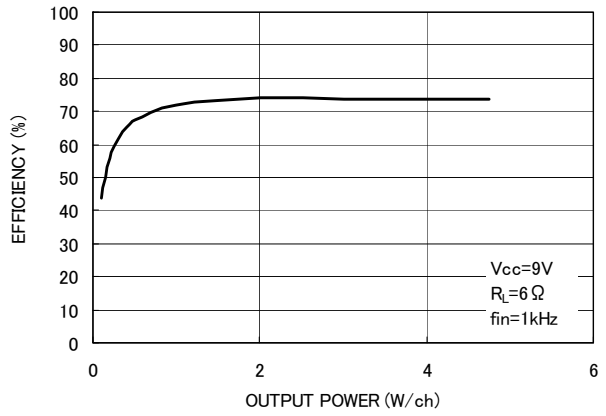


Fig. 21 Output Power - Supply Voltage

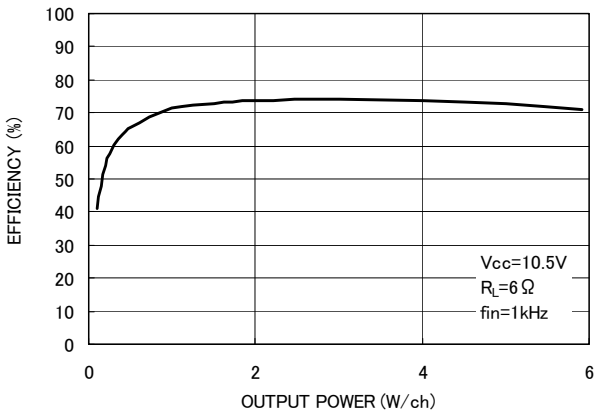


Fig. 22 Efficiency - Output Power

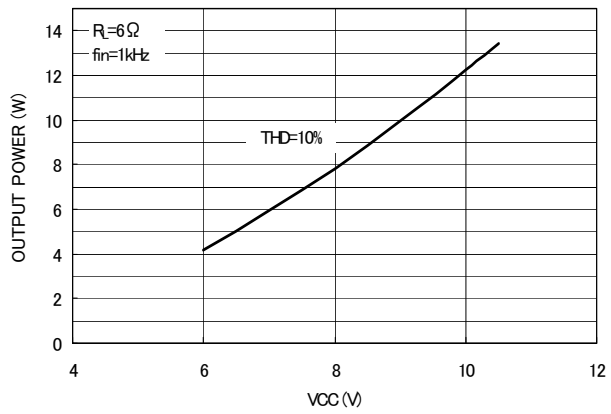


Fig. 23 Efficiency - Output Power

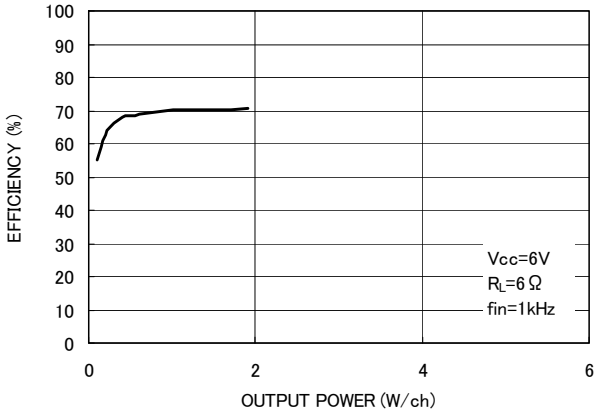


Fig. 24 Efficiency - Output Power

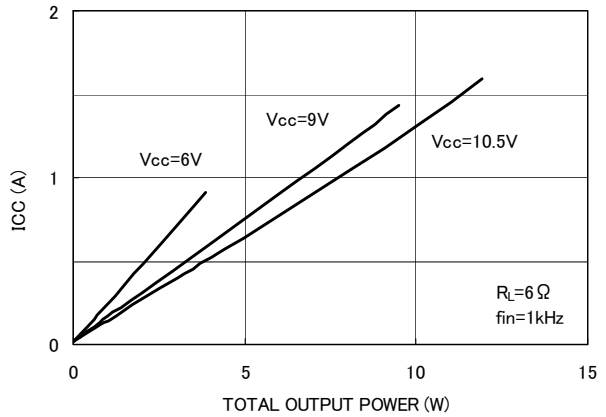


Fig. 25 Current Consumption - Output Power

●Pin Assignment Diagram

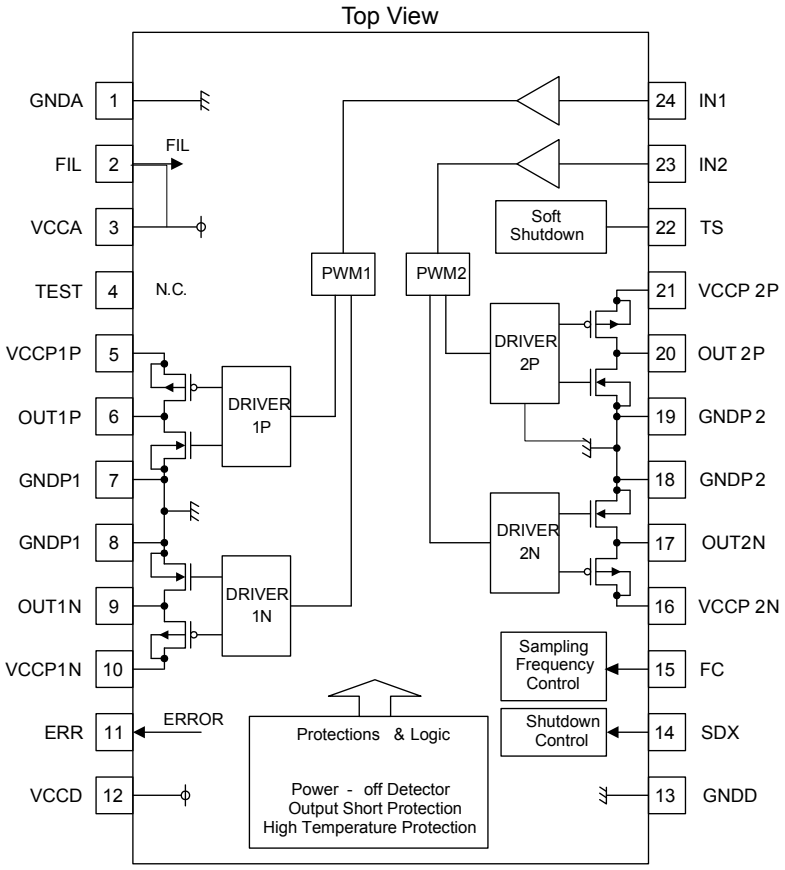


Fig. 26 Pin Assignment

●Outer Dimensions and Inscriptions

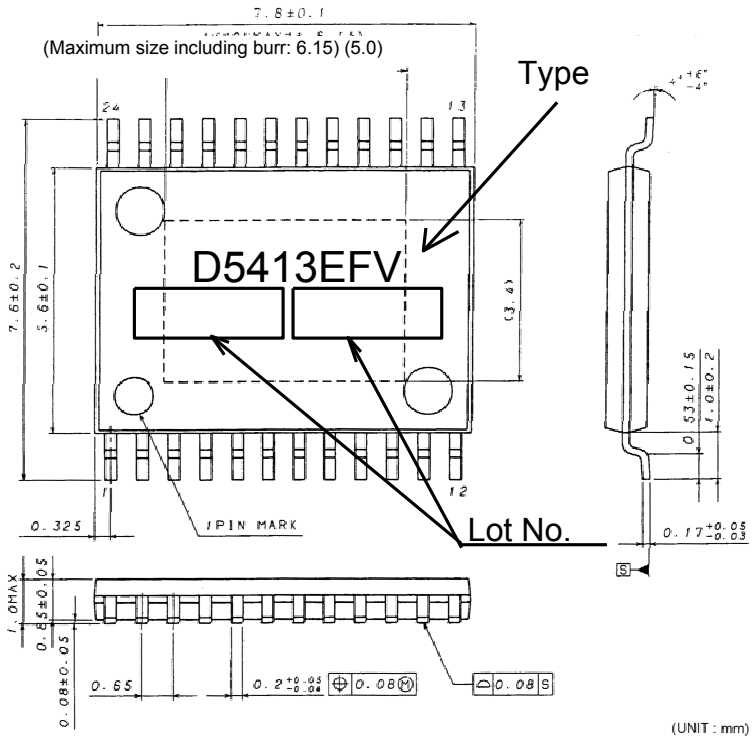
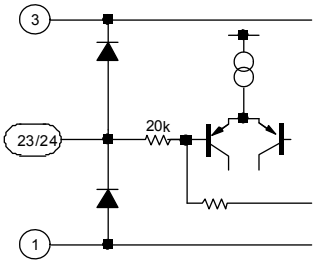
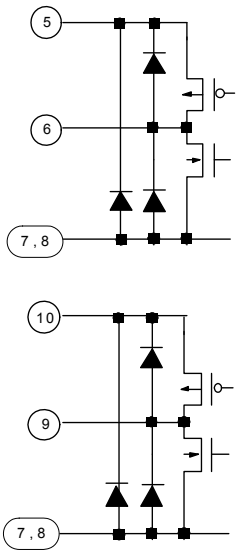
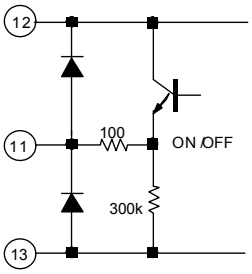
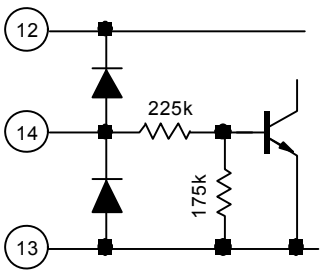
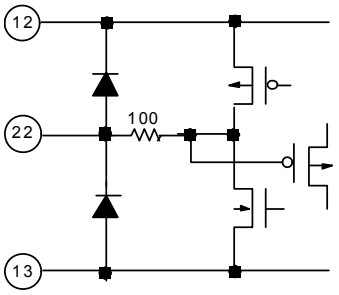
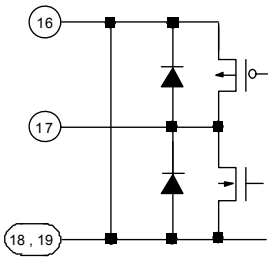
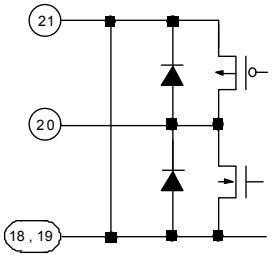
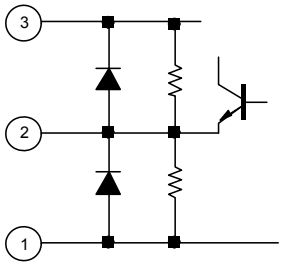


Fig. 27 Outer Dimensions and Inscriptions of the HTSSOP-B24 Package

●**Pin configuration (Pin Voltage: Typical Value)**

No.	Symbol	Pin voltage	Pin description	Internal equalizing circuit
24 23	IN1 IN2	1/2Vcc	ch1: Analog signal input pin ch2: Analog signal input pin Input an audio signal via a capacitor.	
5	VCCP1P	Vcc	ch1: Positive power system power supply pin	
6	OUT1P	Vcc to 0V	ch1: Positive PWM signal output pin Make connection to the output LPF.	
7, 8	GNDP1	0V	ch1: Power GND pin	
9	OUT1N	Vcc to 0V	ch1: Negative PWM signal output pin Make connection to the output LPF.	
10	VCCP1N	Vcc	ch1: Negative power system power supply pin	
11	ERROR	H: 5V L: 0V	Error output pin Pin for notifying an operation error H: Error L: Normal operation	
12	VCCD	Vcc	Control power supply pin	
13	GNDD	0V	Control GND pin	
14	SDX	-	Shut-down control pin H: Shut-down OFF L: Shut-down ON	

●**Pin configuration - Continued**

No.	Symbol	Pin voltage	Pin description	Internal equalizing circuit
4	TEST	VCC	Do not use the TEST pin. Keep this pin open or connect it to VCC for regular use.	
22	TS	0 to 4V	Shut-down ON/OFF Constant setting pin Connect a capacitor.	
16	VCCP2N	Vcc	ch2: Negative power system power supply pin	
17	OUT2N	Vcc to 0V	ch2: Negative PWM signal output pin Make connection to the output LPF.	
18, 19	GNDP2	0V	ch2: Power GND pin	
20	OUT2P	Vcc to 0V	ch2: Positive PWM signal output pin Make connection to the output LPF.	
21	VCCP2P	Vcc	ch2: Positive power system power supply pin	
3	VCCA	Vcc	Analog system power supply pin	
2	FILA	1/2VCC	Analog signal system bias pin Connect a capacitor.	
1	GNDA	0V	Analog signal system GND pin	

●Application Circuit Diagram

(1)Application Circuit Diagram with a Load of 8Ω for Stereo Operation

・Vcc=6V to 10.5V

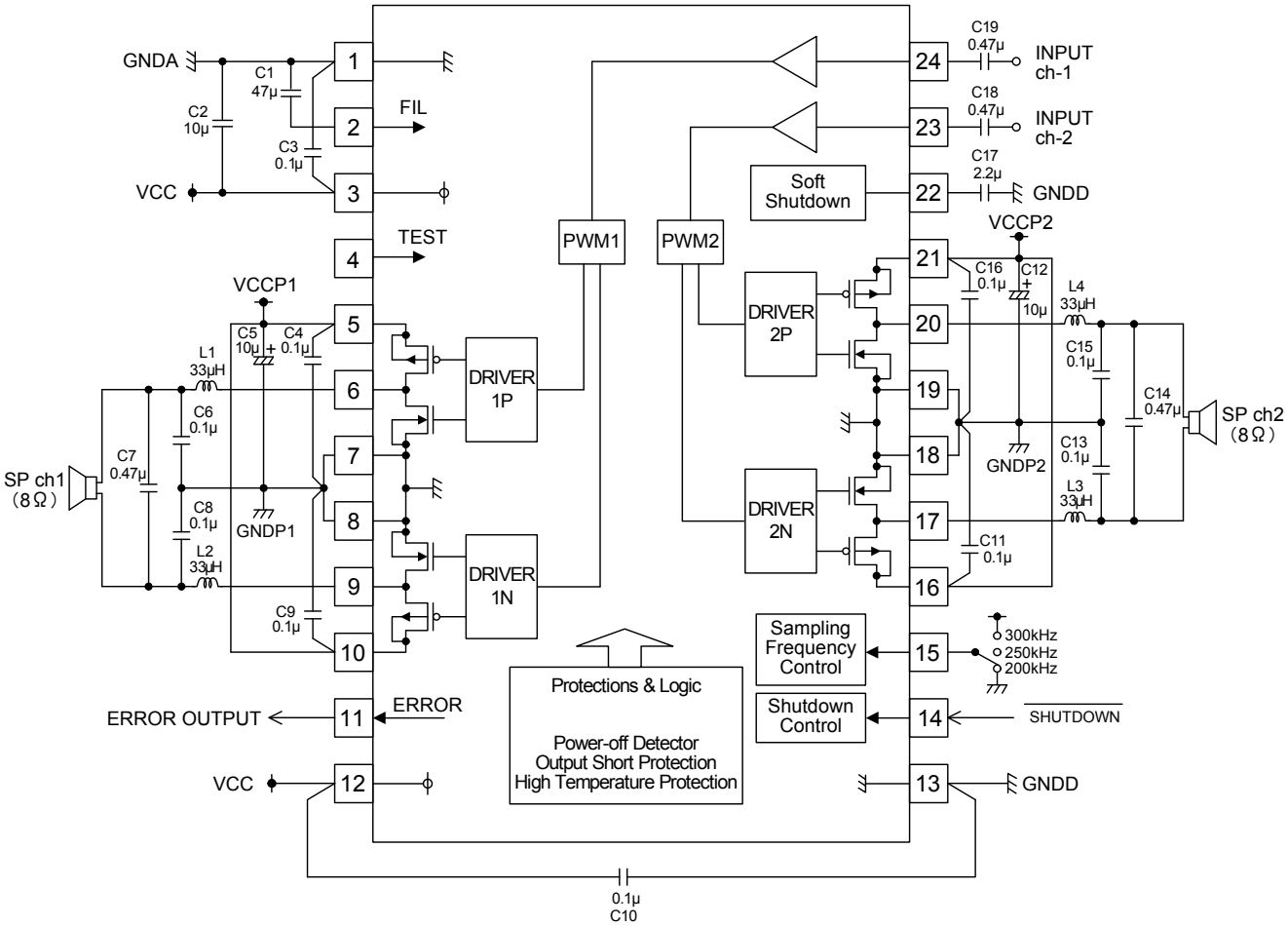


Fig.28 Circuit Diagram with a Load of 8Ω for Stereo Operation

(2)BOMs of Boards for Stereo Operation

Table 1 BOMs of Boards with Loads of 8Ω, 6Ω and 16Ω for Stereo Operation

No.	Item	Part Number	Vendor	Configuration		Value	Rated voltage	Tolerance	Temperature characteristics	Quantity	Reference
				mm	inch						
1	IC	BD5413EFV	ROHM	HTSSOP-B24		-	-	-	-	1	IC1
2	C	GRM32EB31A476KE20	MURATA	3225	1210	47μF	10V	±10%	±10%	1	C1
3	C	GRM21BB31C106KE15	MURATA	2012	0805	10μF	16V	±10%	±10%	1	C2
4	C	GRM188B11C104KA01	MURATA	1608	0603	0.1μF	16V	±10%	±10%	6	C3, C4, C9, C10, C11, C16
5	C	GRM188B30J225KE18	MURATA	1608	0603	2.2μF	6.3V	±10%	±10%	1	C17
6	C	GRM188B11C474KA87	MURATA	1608	0603	0.47μF	16V	±10%	±10%	2	C18, C19
7	C	EMZA350ADA100ME61G	CHEM1-00N	5.3×5.3		10μF	35V	±20%	+20%, -25%	2	C5, C12

BOM of Board with a Load Resistance of 8Ω

No.	Item	Part Number	Vendor	Configuration		Value	Rated voltage	Tolerance	Temperature characteristics	Quantity	Reference
				mm	inch						
8	C	GRM188B11C104KA01	MURATA	1608	0603	0.1μF	16V	±10%	±10%	4	C6, C8, C13, C15
9	C	GRM188B11C474KA87	MURATA	1608	0603	0.47μF	16V	±10%	±10%	2	C7, C14

No.	Item	Part Number	Vendor	Configuration	Value	Tolerance	DC Resistance	Rated DC Current	Quantity	Reference
				mm						
10	L	TSL0808RA-330K1R4-PF	TDK	Φ8.5, 8.3	33μH	±10%	92mΩmax	1.4A max	4	L1, L2, L3, L4

BOM of Board with a Load Resistance of 6Ω

No.	Item	Part Number	Vendor	Configuration		Value	Rated voltage	Tolerance	Temperature characteristics	Quantity	Reference
				mm	inch						
8	C	GRM188B11C474KA87	MURATA	1608	0603	0.47μF	16V	±10%	±10%	4	C6, C8, C13, C15
9	C	GRM188B11C474KA87	MURATA	1608	0603	0.47μF	16V	±10%	±10%	2	C7, C14

No.	Item	Part Number	Vendor	Configuration	Value	Tolerance	DC Resistance	Rated DC Current	Quantity	Reference
				mm						
10	L	TSL0808RA-220K1R7-PF	TDK	Φ8.5, 8.3	22μH	±10%	70mΩmax	1.7A max	4	L1, L2, L3, L4

BOM of Board with a Load Resistance of 16Ω

No.	Item	Part Number	Vendor	Configuration		Value	Rated voltage	Tolerance	Temperature characteristics	Quantity	Reference
				mm	inch						
8	C	GRM188B11C104KA01	MURATA	1608	0603	0.01μF	16V	±10%	±10%	4	C6, C8, C13, C15
9	C	GRM188B11C224KA01	MURATA	1608	0603	0.22μF	16V	±10%	±10%	2	C7, C14

No.	Item	Part Number	Vendor	Configuration	Value	Tolerance	DC Resistance	Rated DC Current	Quantity	Reference
				mm						
10	L	TSL0808RA-680K1R0-PF	TDK	Φ8.5, 8.3	68μH	±10%	160mΩmax	1A max	4	L1, L2, L3, L4

●Notes for use

1. About absolute maximum ratings
   If an applied voltage or an operating temperature exceeds an absolute maximum rating, it may cause destruction of a device. A result of destruction, whether it is short mode or open mode, is not predictable. Therefore, provide a physical safety measure such as fuse, against a special mode that may violate conditions of absolute maximum ratings.

2. About power supply line
   As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as a electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

3. Potential of GND (1, 7, 8, 13, 18 and 19 pins)
   Potential of the GND terminal must be the lowest under any operating conditions.

4. About thermal design
   Perform thermal design with sufficient margins, in consideration of maximum power dissipation Pd under actual operating conditions. This product has an exposed frame on the back of the package, and it is assumed that the frame is used with measures to improve efficiency of heat dissipation. In addition to front surface of board, provide a heat dissipation pattern as widely as possible on the back also.
   A class-D power amplifier has heat dissipation efficiency far higher than that of conventional analog power amplifier and generates less heat. However, extra attention must be paid in thermal design so that a power dissipation Pdiss should not exceed the maximum power dissipation Pd.

Maximum power dissipation	$Pd = Po\frac{Tjmax - Ta}{\theta ja}$ [W]	Tjmax: Maximum temperature junction = 150[℃] Ta: Operating ambient temperature [℃] θja: Package thermal resistance [℃/W] Po: Output power [W] η: Efficiency
Power dissipation	$Pdiss = Po\left(\frac{1}{\eta} - 1\right)$ [W]	

5. About operations in strong electric field
   Note that the device may malfunction in a strong electric field.

6. Thermal shutdown (TSD) circuit
   This product is provided with a built-in thermal shutdown circuit. When the thermal shutdown circuit operates, the output transistors are placed under open status. The thermal shutdown circuit is primarily intended to shut down the IC avoiding thermal runaway under abnormal conditions with a chip temperature exceeding Tjmax = 150℃, and is not intended to protect and secure an electrical appliance. Accordingly, do not use this circuit function to protect a customer's electrical appliance.

7. About shorting between pins and installation failure
   Be careful about direction and displacement of an IC when installing it onto the board. Faulty installation may destroy the IC when the device is energized. In addition, a foreign matter getting in between IC pins, pins and power supply, and pins and GND may cause shorting and destruction of the IC.

8. About power-on or power-off sequence
   Set the SDX pin (pin 14) to “L” level before initiating the power-on sequence. Similarly, set the SDX pin (pin 14) to “L” level before initiating the power-off sequence. If such a setting is made, pop reduction is achieved at power-on or power-off sequence. In addition, note that all power supply pins shall be made active or inactive at the same time.

9. About error output pin (pin 11)
   When a high temperature protection function or VCC/GND shorting protection function is activated, an error flag is output via an error output pin. Because the error output pin is primarily intended to indicate the state of BD5413EFV and is available only to protect BD5413EFV, it cannot be used for any other purposes.

10. About TEST pin (pin 4)
    Do not use the TEST pin. Keep this pin open or connect it to VCC for regular use.

●Ordering part number

B	D	5	4	1	3	E	F	V	-	E	2

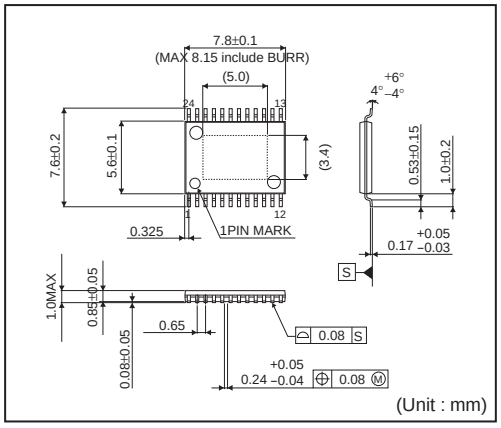
Part No
BD.

Part No.
5413

Package
EFV:HTSSOP-B24

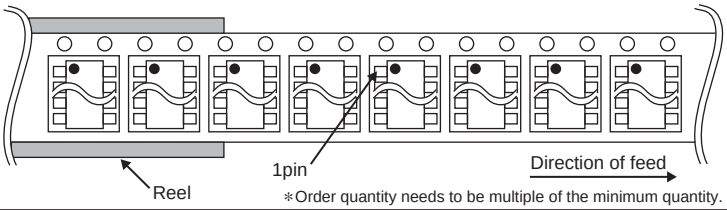
Packaging and forming specification
E2: Embossed tape and reel

HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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