

- 1.TYPE RZE002P02
 2.STRUCTURE SILICON P-CHANNEL MOS FET
 3.APPLICATIONS SWITCHING
 4.ABSOLUTE MAXIMUM RATINGS [Ta=25°C]

DRAIN-SOURCE VOLTAGE		V_{DSS}	• • •	-20V
GATE-SOURCE VOLTAGE		V_{GSS}	• • •	±10V
DRAIN CURRENT	CONTINUOUS	I_D	• • •	±200mA
	PULSED	I_{DP}	• • •	±800mA PW ≤ 10 μs DUTY CYCLE ≤ 1%
SOURCE CURRENT	CONTINUOUS	I_S	• • •	-100mA
(BODY DIODE)	PULSED	I_{SP}	• • •	-800mA PW ≤ 10 μs DUTY CYCLE ≤ 1%
TOTAL POWER DISSIPATION		P_D	• • •	150mW EACH TERMINAL MOUNTED ON A RECOMMENDED LAND
CHANNEL TEMPERATURE		T_{ch}	• • •	150°C
RANGE OF STORAGE TEMPERATURE		T_{stg}	• • •	-55~150°C

5.THERMAL RESISTANCE

CHANNEL TO AMBIENT	$R_{th(ch-a)}$	• • •	833°C/W EACH TERMINAL MOUNTED ON A RECOMMENDED LAND
--------------------	----------------	-------	---

DESIGN <i>J. Mizusaki</i>	CHECK <i>A. Tsubaki</i>	APPROVAL <i>T. Komaki</i>	DATE : 05/JAN/2009	SPECIFICATION No. TSQ03037H-RZE002P02
			REV. : 0	ROHM Co.,Ltd.

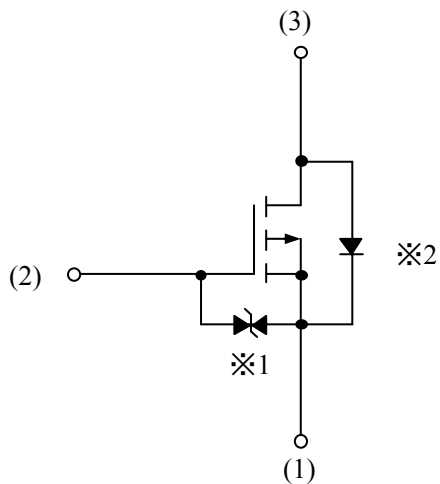
6.ELECTRICAL CHARACTERISTICS [Ta=25 °C]

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
GATE-SOURCE LEAKAGE	I_{GSS}	$V_{GS}=\pm 10V/V_{DS}=0V$	—	—	$\pm 10 \mu A$
DRAIN-SOURCE BREAKDOWN VOLTAGE	$V_{(BR)DSS}$	$I_D=-1mA/V_{GS}=0V$	-20V	—	—
ZERO GATE VOLTAGE DRAIN CURRENT	I_{DSS}	$V_{DS}=-20V/V_{GS}=0V$	—	—	-1 μA
GATE THRESHOLD VOLTAGE	$V_{GS(th)}$	$V_{DS}=-10V/I_D=-100\mu A$	-0.3V	—	-1.0V
STATIC DRAIN-SOURCE ON-STATE RESISTANCE	$R_{DS(on)}$ * PULSED	$I_D=-200mA / V_{GS}=-4.5V$	—	0.8 Ω	1.2 Ω
		$I_D=-100mA / V_{GS}=-2.5V$	—	1.0 Ω	1.5 Ω
		$I_D=-100mA / V_{GS}=-1.8V$	—	1.3 Ω	2.2 Ω
		$I_D=-40mA / V_{GS}=-1.5V$	—	1.6 Ω	3.5 Ω
		$I_D=-10mA / V_{GS}=-1.2V$	—	2.4 Ω	9.6 Ω
FORWARD TRANSFER ADMITTANCE	$ Y_{fs} $ * PULSED	$V_{DS}=-10V/I_D=-200mA$	0.2S	—	—
INPUT CAPACITANCE	C_{iss}	$V_{DS}=-10V$ $V_{GS}=0V$ $f=1MHz$	—	115pF	—
OUTPUT CAPACITANCE	C_{oss}		—	10pF	—
REVERSE TRANSFER CAPACITANCE	C_{rss}		—	6pF	—
TURN-ON DELAY TIME	$t_{d(on)}$ * PULSED	$V_{DD} \doteq -10V$ $I_D=-100mA$ $V_{GS}=-4.5V$ $R_L \doteq 100 \Omega$ $R_G=10 \Omega$ See Fig 1-1.1-2	—	6ns	—
RISE TIME	t_r * PULSED		—	4ns	—
TURN-OFF DELAY TIME	$t_{d(off)}$ * PULSED		—	17ns	—
FALL TIME	t_f * PULSED		—	17ns	—
TOTAL GATE CHARGE	Q_g * PULSED	$V_{DD} \doteq -10V$ $I_D=-200mA$ $V_{GS}=-4.5V$ $R_L \doteq 50 \Omega / R_G=10 \Omega$ See Fig 2-1.2-2	—	1.4nC	—
GATE-SOURCE CHARGE	Q_{gs} * PULSED		—	0.3nC	—
GATE-DRAIN CHARGE	Q_{gd} * PULSED		—	0.3nC	—

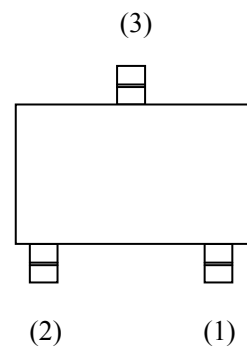
BODY DIODE CHARACTERISTICS (SOURCE-DRAIN)

PARAMETER	ITEM	CONDITION	MIN.	TYP.	MAX.
FORWARD VOLTAGE	V_{SD} * PULSED	$I_S=-200mA/V_{GS}=0V$	—	—	-1.2V

7. INNER CIRCUIT

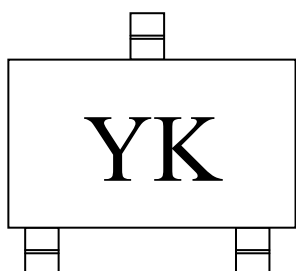


(1)SOURCE
(2)GATE
(3)DRAIN



※ 1 ESD PROTECTION DIODE
※ 2 BODY DIODE

8. MARKING



“YK ” MEANS RZE002P02.

9.MEASUREMENT CIRCUIT

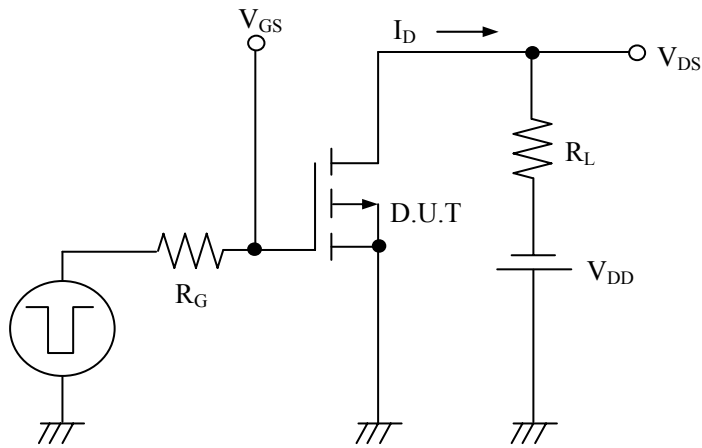


Fig.1-1 SWITCHING TIME MEASUREMENT CIRCUIT

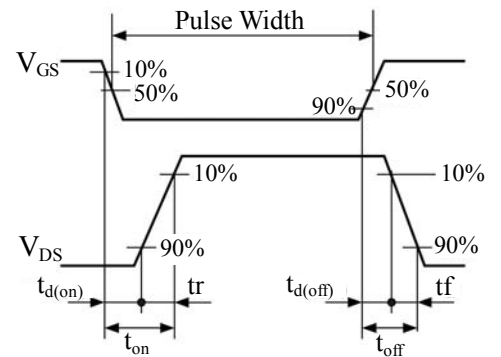


Fig.1-2 SWITCHING WAVEFORMS

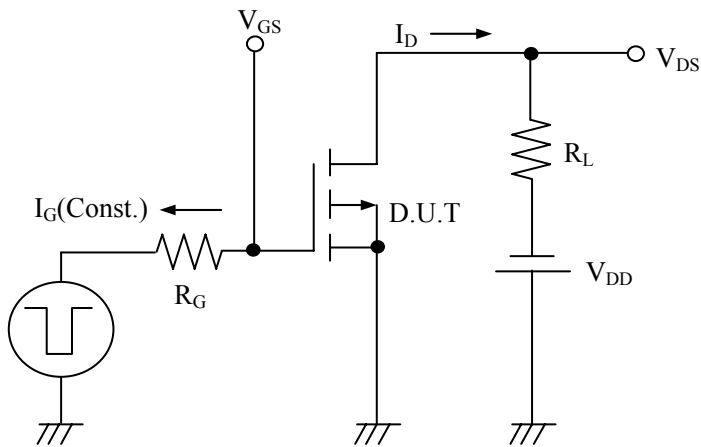


Fig.2-1 GATE CHARGE MEASUREMENT CIRCUIT

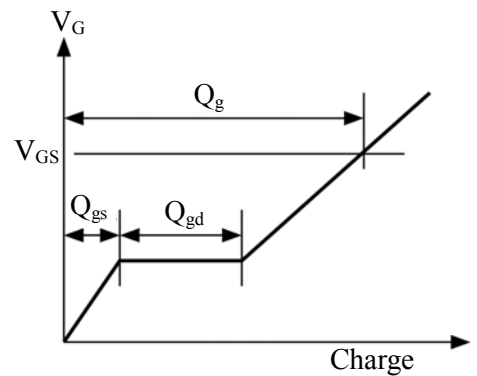


Fig.2-2 GATE CHARGE WAVEFORM

10.Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.