Structure Silicon monolithic integrated circuit

Product Name SDTV signal to HDTV signal Up Converter LSI for Camcorder

Type **BU1521GVW**

Function
- Input format
  480i or 576i(ITUR BT656) YCbCr 4:2:2(ITUR BT601) 8bit Digital Interface
- Output format
  480i or 576i(ITUR BT656) YCbCr 4:2:2 8bit Digital Interface
  480p or 576p(SMPTE 293・ITUR BT1358) YCbCr 4:2:2 16bit Digital Interface
  1080/59.94i(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
  1080/50i(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
  1080/59.94p(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
  1080/50p(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
- IP conversion function
- Up scale function
- Five taps coefficient variable filter function
- Register access by SPI interface
- Built-in PLL(Output frequency : 74.25MHz,74.175824MHz,148.5MHz,148.351648MHz)

## ○ Absolute maximum ratings

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Power supply voltage 1 (SD input) | VDDIO1 | -0.3～+4.2 | V |
| Power supply voltage 2 (Control) | VDDIO2 | -0.3～+4.2 | V |
| Power supply voltage 3 (HD output) | VDDIO3 | -0.3～+4.2 | V |
| Power supply voltage 4 (PLL) | AVDD | -0.3～+4.2 | V |
| Power supply voltage 5 (CORE) | VDD | -0.3～+1.68 | V |
| Input voltage 1 | VIN1 | -0.3～VDDIO1+0.3 | V |
| Input voltage 2 | VIN2 | -0.3～VDDIO2+0.3 | V |
| Input voltage 3 | VIN3 | -0.3～VDDIO3+0.3 | V |
| Storage temperature range | Tstg | -25～+125 | ºC |
| Power dissipation | PD | 330 *1, 1200 *2 | mW |

*1 IC only. In the case of exceeding 25°C, 3.3 mW should be reduced at the rating 1°C.
*2 When packaging a glass epoxy board of 114.3x76.2x1.6mm. If exceeding 25°C, 12mW should be reduced at the rating 1°C.
* Has not been designed to withstand radiation.

## ○ Recommended operating conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltage 1 (SD input) | VDDIO1 | 1.7 | 3.3 | 3.6 | V |
| Power supply voltage 2 (Control) | VDDIO2 | 2.7 | 3.0 | 3.3 | V |
| Power supply voltage 3 (HD output) | VDDIO3 | 1.7 | 1.8 | 1.9 | V |
| Power supply voltage 4 (PLL) | AVDD | 2.7 | 3.0 | 3.3 | V |
| Power supply voltage 5 (CORE) | VDD | 1.15 | 1.2 | 1.25 | V |
| Operating temperature range | Topr | -25 | - | 85 | ℃ |

Status of this document
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Application example
- ROHM cannot provide adequate confirmation of patents.
- The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
  Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.
- ROHM assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

○ Electric characteristics

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Operating current (CORE) | IDD1 | - | 150 | 200 | mA | CLKOUT=148.5MHz |
| Operating current (IO) | IDD2 | - | 40 | 80 | mA | CLKOUT=148.5MHz, Load capacitance=5pF |
| Operating current (CORE) | IDD3 | - | 15 | 20 | mA | CLKOUT=27MHz |
| Operating current (IO) | IDD4 | - | 10 | 20 | mA | CLKOUT=27MHz、Load capacitance=5pF |
| Static consumption current | IDDst | - | - | 600 | uA | Standby mode |
| Input "H" voltage | IIH | -10 | - | 10 | uA | VIH=VDDIO1/2 |
| Input "L" voltage | IIL | -10 | - | 10 | uA | VIL=GND |
| Input "H" voltage 1 | VIH1 | VDDIO1 *0.8 | - | VDDIO1 +0.3 | V | Normal input (including input mode of I/O terminal) |
| Input "L" voltage 1 | VIL1 | -0.3 | - | VDDIO1 *0.2 | V | Normal input (including input mode of I/O terminal) |
| Input "H" voltage 2 | VIH2 | VDDIO1 *0.85 | - | VDDIO1 +0.3 | V | Hysteresis input (CLKIN) |
| Input "L" voltage 2 | VIL2 | -0.3 | - | VDDIO1 *0.15 | V | Hysteresis input (CLKIN) |
| Input "H" voltage 3 | VIH3 | VDDIO2 *0.85 | - | VDDIO2 +0.3 | V | Hysteresis input (RESETB,SCLK,SCSB) |
| Input "L" voltage 3 | VIL3 | -0.3 | - | VDDIO2 *0.15 | V | Hysteresis input (RESETB,SCLK,SCSB) |
| Output "H" voltage 1 | VOH1 | VDDIO2 -0.4 | - | VDDIO2 | V | IOH1=-1.0mA(DC) SDOUT |
| Output "L" voltage 1 | VOL1 | 0.0 | - | 0.4 | V | IOL1=1.0mA(DC) SDOUT |
| Output "H" voltage 2 | VOH2 | VDDIO3 -0.2 | - | VDDIO3 | V | IOH1=-1.0mA(DC) HD output pin |
| Output "L" voltage 2 | VOL2 | 0.0 | - | 0.2 | V | IOL1=1.0mA(DC) HD output pin |

(Unless otherwise specified,VDD=1.20V,VDDIO1=3.3V, VDDIO3=1.8V,VDDIO2=AVDD=3.0V,AVSS=GND=0.0V,Ta=25°C)

○ Output frequency list (CLKIN input frequency =27.000000MHz、when a system use internal PLL)

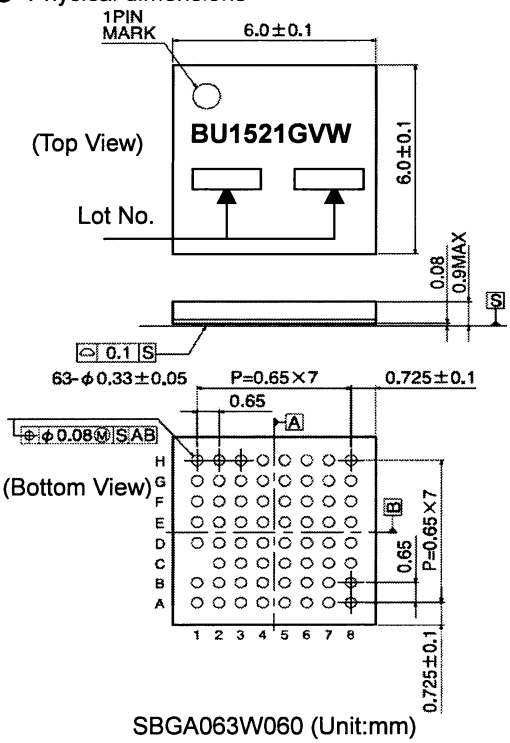
| Output format | CLKOUT(MHz) |
|---|---|
| 1080/59.94i | 74.175824 |
| 1080/50i | 74.250000 |
| 1080/59.94p | 148.351648 |
| 1080/50p | 148.500000 |

When in the 480i/576i output format mode, the input clock 27MHz is put out the CLKOUT pin without internal PLL processing

## O Pin Function Descriptions

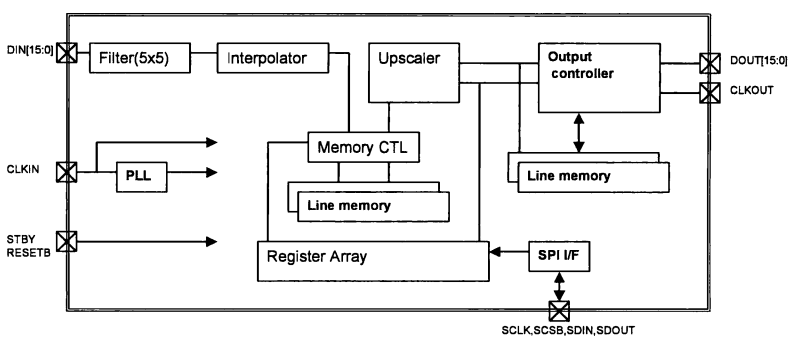
| PIN No | PIN Name | Descriptions | PIN No | PIN Name | Descriptions |
|---|---|---|---|---|---|
| B2 | DI3 | SD input data 3bit | G7 | DO0 | HD output data 0bit |
| D4 | AVDD | Power supply for PLL(TYP3.0V) | E5 | VDDIO3 | Output data side IO voltage (TYP1.8V) |
| B1 | DI6 | SD input data 6bit | G8 | DO2 | HD output data 2bit |
| C2 | DI5 | SD input data 5bit | F7 | DO4 | HD output data 4bit |
| C1 | N.C | With no ball | F8 | DO3 | HD output data 3bit |
| D3 | VDDIO1 | Input data side IO voltage (TYP3.3V) | E6 | GND | GND |
| D2 | DI12 | SD input data 12bit | E7 | DO6 | HD output data 6bit |
| D1 | DI9 | SD input data 9bit | E8 | DO5 | HD output data 5bit |
| E1 | DI14 | SD input data 14bit | D8 | DO7 | HD output data 7bit |
| E2 | DI0 | SD input data 0bit | D7 | DO8 | HD output data 8bit |
| E3 | GND | GND | D6 | VDD | Core power supplly (TYP1.2V) |
| F1 | DI10 | SD input data 10bit | C8 | DO9 | HD output data 9bit |
| F2 | DI7 | SD input data 7bit | C7 | DO10 | HD output data 10bit |
| G1 | DI13 | SD input data 13bit | B8 | DO11 | HD output data 11bit |
| F3 | GND | GND | C6 | GND | GND |
| H1 | GND | GND | A8 | GND | GND |
| G2 | DI11 | SD input data 11bit | B7 | DO12 | HD output data 12bit |
| E4 | VDD | Core power supply(TYP1.2V) | D5 | GND | GND |
| H2 | DI15 | SD input data 15bit | A7 | DO13 | HD output data 13bit |
| G3 | DI2 | SD input data 2bit | B6 | DO14 | HD output data 14bit |
| H3 | DI1 | SD input data 1bit | A6 | DO15 | HD output data 15bit |
| F4 | RESETB | Reset pin (Low active) | C5 | VDDIO3 | Output data side IO voltage (TYP1.8V) |
| G4 | SCLK | 3 line type serial I/F clock | B5 | TEST0 | Test pin 0(Please connect iwith GND.) |
| H4 | SCSB | 3 line type seria I/Fchip select | A5 | TEST1 | Test pin 1(Please connect iwith GND.) |
| H5 | SDIN | 3 line type serial I/F input data | A4 | TEST2 | Test pin 2(Please connect iwith GND) |
| G5 | SDOUT | 3 line type serial I/F output data | B4 | GND | GND |
| F5 | VDDIO2 | Control signal IO voltage (TYP3.0V) | C4 | AVSS | GND for PLL |
| H6 | STBY | IC standby control | A3 | CLKIN | SD clock input(27MHz) |
| G6 | CLKOUT | HD clock output | B3 | DI8 | SD data input 8bit |
| H7 | DO1 | HD output data 1bit | A2 | DI4 | SD data input 4bit |
| F6 | VDD | Core power supplly (TYP1.2V) | C3 | GND | GND |
| H8 | GND | GND | A1 | GND | GND |

## O Physical dimensions




SBGA063W060 (Unit:mm)

## O Block diagram



O Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.