

Structure	Silicon Monolithic Integrated Circuit
Product name	Coupling Capacitorless Stereo Headphone Amp IC
Type	BD88415GUL
Package outline	Fig.1 Package outline
Block diagram	Fig.2 Block diagram
Function	<ul style="list-style-type: none"> • 2.4V to 4.5V Single-Supply Operation • No Bulky DC-Blocking Capacitors Required • No Degradation of Low-Frequency Response Due to Output Capacitors • Ground-Referenced Outputs • Fixed Gain(Av=-1.5) • Integrated Negative Power Supply • Low THD+N • Short-Circuit and Thermal-Overload Protection

○Absolute Maximum Ratings

Parameter	Symbol	Rating	Parameter
SGND to PGND voltage	Vgg	0	V
SVDD to PVDD voltage	Vdd	-0.3~+0.3	V
SVSS to PVSS voltage	Vss	0	V
SGND or PGND to SVDD, PVDD voltage	Vdg	-0.3~6	V
SVSS, PVSS to SGND or PGND voltage	Vsg	-6~+0.3	V
SGND to IN_ - voltage	Vin	-2.8~2.8	V
SGND to OUT_ - voltage	Vout	-2.8~2.8	V
PGND to C1P- voltage	Vc1p	(PGND-0.3)~(PVDD+0.3)	V
PGND to C1N- voltage	Vc1n	(PVSS-0.3)~(PGND+0.3)	V
SGND to SHDN_ - voltage	Vsh	(SGND-0.3)~(SVDD+0.3)	V
Input current	Iin	-10~10	mA
Power Dissipation	Pd	T.B.D.	mW
Storage Temperature Range	Tstg	-55~+125	deg

○Recommended operating range

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Supply Voltage	VDD	2.4	-	4.5	V
Operation Temperature Range	Topr	-40	-	+85	deg

© This chip is not designed to protect itself against radioactive rays.

Status of this document:

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Attention:

These specifications are not guaranteed because of target specification. And the specifications are subject to change without notice.

○Electrical characteristics

Unless otherwise specified

Ta=25deg, PVDD=SVDD=3.3V, PGND=SGND=0V, SHDNB=SVDD, C1=C2=2.2uF, RL=no load

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Current consumption						
Standby Current	IST	-	0.1	2	uA	SHDNLB=SHDNRB=L
Operating Current	IDD1	-	1.9	-	mA	SHDNLB=H, SHDNRB=L, no signal, RL=no load
	IDD2	-	3.0	7.4	mA	SHDNLB=SHDNRB=H, no signal, RL=no load
SHDNL/RB_Terminal						
H Level Input Voltage	VIH	1.95	-	-	V	
L Level Input Voltage	VIL	-	-	0.7	V	
Input Leak Current	IIN	-	-	±1	uA	
Headphone amp						
Full Operation Time	tSON	-	80	-	us	SHDNLB, SHDNRB L→H
Offset Voltage	VIS	-	±0.5	±4.0	mV	
Output Power	POUT	30	50	-	mW	RL=32ohm, THD+N ≤ -40dB
		40	80	-	mW	RL=16ohm, THD+N ≤ -40dB
THD+N	THD+N	-	-80	-65	dB	RL=32ohm, POUT=10mW, f=1kHz, 20kHz - LPF
		-	-75	-60	dB	RL=16ohm, POUT=10mW, f=1kHz, 20kHz - LPF
Input Impedance	ZIN	10	14	19	kohm	SHDNxB=L
Gain	AV	-1.55	-1.5	-1.45	V/V	
Gain match	ΔAV	-	1	-	%	
Noise	VN	-	-100	-	dBV	20kHz LPF+JIS-A
Slew Rate	SR	-	0.15	-	V/us	
Maximum Capacitive Load	CL	-	200	-	pF	
Crosstalk	SP	-	-80	-	dB	RL=32Ω, f=1kHz, VOUT=200mV _{P-P} , 1kHz BPF
PSRR	PSRR	-	-80	-	dB	f=217Hz, 100mV _{P-P} - ripple
Charge-Pump Oscillator Frequency	fOSC	234	320	459	kHz	
Thermal-Shutdown Threshold	TSD	-	145	-	deg	
Thermal-Shutdown Hysteresis	-	-	5	-	deg	

※ The values indicated in headphone part are for single channel.

○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) About the rush current

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

(13) Others

In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functional description, Application note.