

STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCT NAME Overvoltage Protection Controller with Internal FET

MODEL NAME **BD6040GUL**

FEATURES

- Overvoltage Protection up to 28V
- Internal Low Ron (125mΩ) FET
- Over voltage Lockout (OVLO)
- Under voltage Lockout(UVLO)
- Internal 2msec Startup Delay
- Over Current Protect
- Thermal Shut Down
- Small package: VCSP50L1(1.6mm x 1.6mm, height=0.55mm)

● Absolute maximum ratings (Ta=25°C)

| Contents | Symbol | Rating | Unit | Conditions |
|-----------------------------|--------|----------|------|------------|
| Input supply voltage 1 | Vmax1 | -0.3~30 | V | IN |
| Input supply voltage 2 | Vmax2 | -0.3~7 | V | other |
| Power dissipation | Pd | 725 | mW | |
| Operating temperature range | Topr | -35~+85 | °C | |
| Storage temperature range | Tstr | -55~+150 | °C | |

※1 When using more than at Ta=25°C, it is reduced 5.8 mW per 1°C.
 ROHM specification board 50mm×58mm mounting.

● Recommended operating range (Ta=-35~+85°C)

| Parameter | Symbol | Range | Unit | Usage |
|---------------------|-----------------|--------|------|-------|
| Input voltage range | V _{in} | 2.2~28 | V | |

※ This product is not especially designed to be protected from radioactivity.

Status of this document.

The Japanese version of this document is the formal specification.

A customer may use this translation version only for reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

Application example

The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

| DESIGN | CHECK | APPROVAL | DATE | SPECIFICATION No. |
|-------------|------------------|-----------------|-------------|------------------------|
| 24/Aug/2007 | 24/Aug/2007 | <i>Sachiro</i> | 24/Aug/2007 | TSZ02201-BD6040GUL-1-2 |
| y.tamegai | <i>D. Yokomi</i> | <i>Horiuchi</i> | REV. A | ROHM CO., LTD. |
| | | 24/Aug/07 | | |

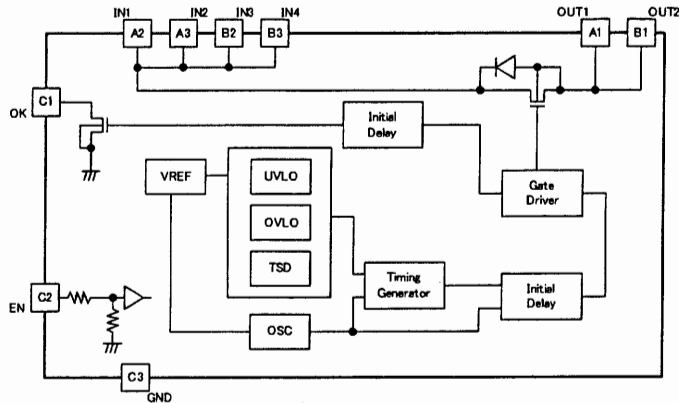
● Electrical Characteristics

(Unless otherwise noted, Ta = 25°C)

| Parameter | Symbol | Rating | | | Unit | Conditions |
|----------------------------------|--------|--------|------|------|------|---------------|
| | | Min. | Typ. | Max. | | |
| ● ELECTRICAL | | | | | | |
| Input Voltage Range | VIN | - | - | 28 | V | |
| Supply Quiescent Current | ICC | | 45 | 90 | μA | |
| Under Voltage Lockout | UVLO | 2.53 | 2.65 | 2.77 | V | IN=decreasing |
| Under Voltage Lockout Hysteresis | UVLOh | 50 | 100 | 150 | mV | IN=increasing |
| Over Voltage Lockout | OVLO | 6.2 | 6.4 | 6.6 | V | IN=increasing |
| Over Voltage Lockout Hysteresis | OVLOh | 10 | 30 | 50 | mV | IN=decreasing |
| Current limit | ILM | 1.2 | - | - | A | |
| Vin vs. Vout Res. | RON | - | 125 | 150 | mΩ | |
| OK Output Low Voltage | OKVO | - | - | 400 | mV | SINK=1mA |
| OK Leakage Current | OKleak | - | - | 1 | μA | |
| EN input voltage (H) | ENH | 1.45 | - | - | V | |
| EN input voltage (L) | ENL | - | - | 0.5 | V | |
| EN input current | ENC | 12 | 25 | 50 | μA | EN=1.5V |
| ● TIMINGS | | | | | | |
| Start Up Delay | Ton | - | 2 | 4 | msec | |
| OK Going Up Delay | Tok | - | 10 | 15 | msec | |
| Output Turn Off Time | Toff | - | 2 | 10 | μsec | |
| Alert Delay | Tovp | - | 1.5 | 10 | μsec | |

* This product is not especially designed to be protected from radioactivity.

● Block Diagram



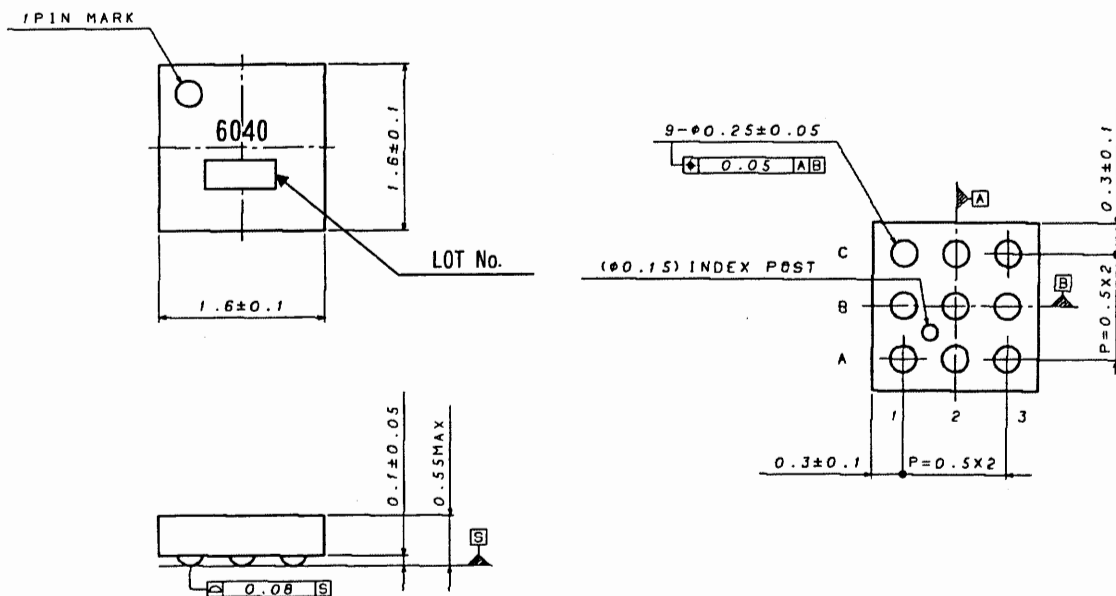
● PIN number/PIN name

| Pin number | Pin name |
|------------|----------|
| A2 | IN1 |
| A3 | IN2 |
| B2 | IN3 |
| B3 | IN4 |
| A1 | OUT1 |
| B1 | OUT2 |
| C3 | GND |
| C1 | OK |
| C2 | EN |

● PIN DESCRIPTIONS

| PIN | NAME | FUNCTION |
|------------------|-----------------|-----------------------------------------------------------------------------------------------------|
| A2, A3 B2, B3 | IN1, 2, 3, 4 | Input voltage Pin. A 1μF low ESR capacitor, or larger must be connected between this pin and GND |
| A1, B1 | OUT1, 2 | Output Voltage Pin |
| C1 | OK | Active-low open drain output to signal if the adapter voltage is correct |
| C3 | GND | Ground Pin |
| C2 | EN | Enable input Drive EN high to turn off OUT (Hi-z output) |

● Package Dimensions (VCSP50L1)



● Use-related Cautions

(1) Absolute maximum ratings

If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)

When junction temperatures become 170°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

— Jisso Information —

Package : VCSP50L1

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1. Structure and materials

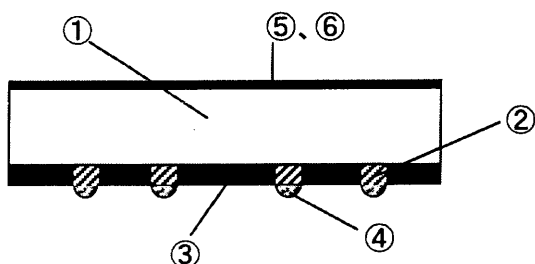


Fig. 1 Structure

| No. | Item | Materials |
|-----|---------------|-----------------------|
| ① | Die | Silicon |
| ② | Cu Post | Cu |
| ③ | Encapsulation | Epoxy Resin |
| ④ | Ext. terminal | Sn-3Ag-0.5Cu Solder |
| ⑤ | Encapsulation | Polyamide-imide Resin |
| ⑥ | Marking | Laser Marking |

Dehydrated weight : 0.003g

2. Tape and Reel information

2. 1. Packing specification

| | |
|-------------------|-----------------------|
| Tape | Embossed carrier tape |
| Quantity | 3,000pcs/Reel |
| Direction of feed | E2 (See Fig. 2) |

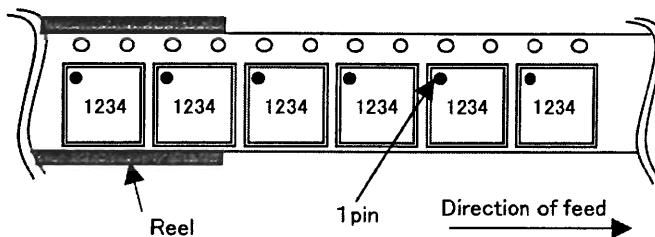


Fig. 2 Typical Tape and Reel configuration

2. 2. Tape and Reel specification

2. 2. 1. Tape and reel dimensions (See the table on page 2/4)

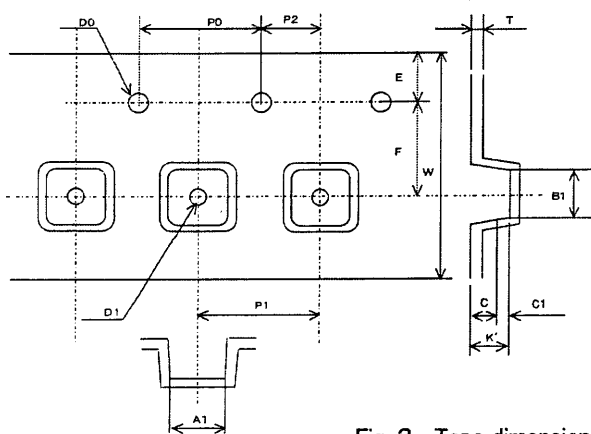


Fig. 3 Tape dimensions

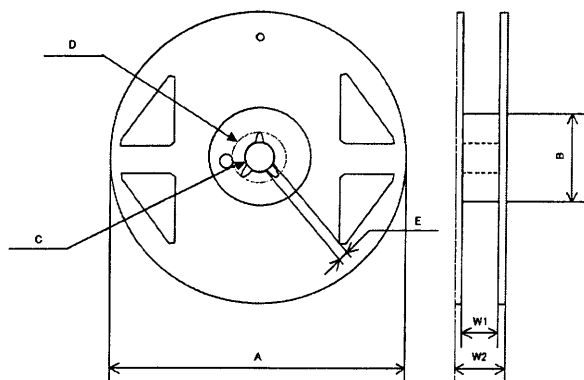


Fig. 4 Reel dimensions

| | | | | |
|------------------------------------|------------------------------------|--------------------------------------------|--------------------|--------------------------------------------|
| DESIGN 24/Aug/2007 y.tamegai | CHECK 24/Aug/2007 D.Yokozono | APPROVAL Sachio Aonishi 24/Aug/07 | DATE: May. 18,2007 | SPECIFICATION No. : TSZ02201-BD6040GUL-1-2 |
| | | | REV. A | ROHM CO.,LTD. |

(Tape dimensions)

| A1 | B1 | C | C1 | D0 | D1 | E | F | K' | P0 | P1 | P2 | T | W |
|--------------|--------------|-------|--------|--------------------|--------------|--------------|-------------|--------------|-------------|-------------|-------------|---------------|-------------|
| 1.87 ±0.1 | 1.87 ±0.1 | (0.6) | (0.25) | Φ1.5 +0.1 -0 | Φ0.8 ±0.1 | 1.75 ±0.1 | 3.5 ±0.1 | 0.85 ±0.1 | 4.0 ±0.1 | 4.0 ±0.1 | 2.0 ±0.1 | 0.30 ±0.05 | 8.0 ±0.3 |

(Reel dimensions)

| A | B | C | D | E | W1 | W2 |
|------|-----------|---------------|--------------|------------|-------------|--------------|
| Φ180 | 50 MIN | Φ13.0 ±0.2 | Φ20.2 MIN | 1.5 MIN | 9.4 ±1.0 | 13.4 ±1.0 |

2. 3. Leader and Trailer

2. 3. 1. Leader

No component pockets are 40 pockets or more.

2. 3. 2. Trailer

No component pockets are 10 pockets or more.

Tape is free from reel.

2. 4. Label for Reel and Box

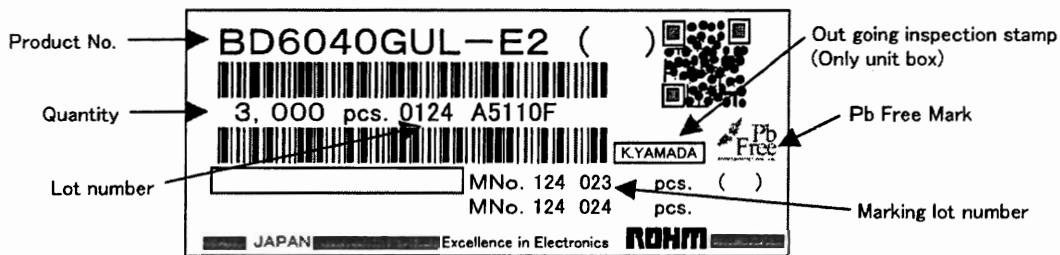


Fig. 5 Label example

2. 5. Packing style

4 reels or less per inner box.

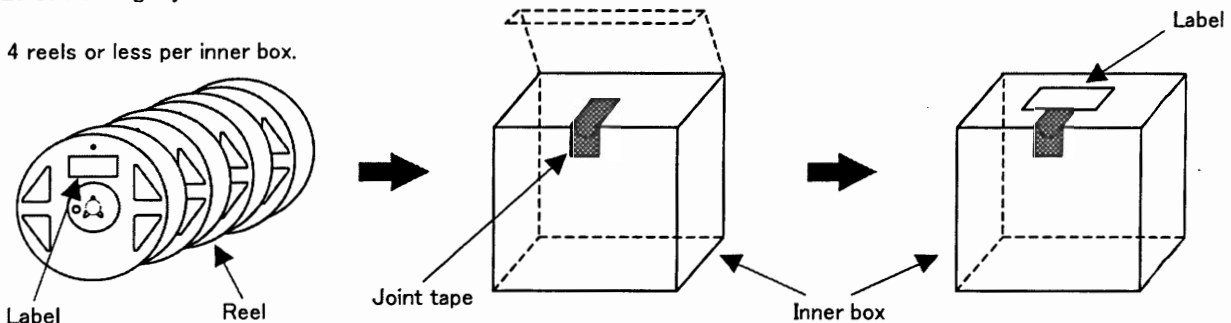


Fig. 6 Packing style

2. 6. Shipping style

4 unit boxes or less per shipping box.

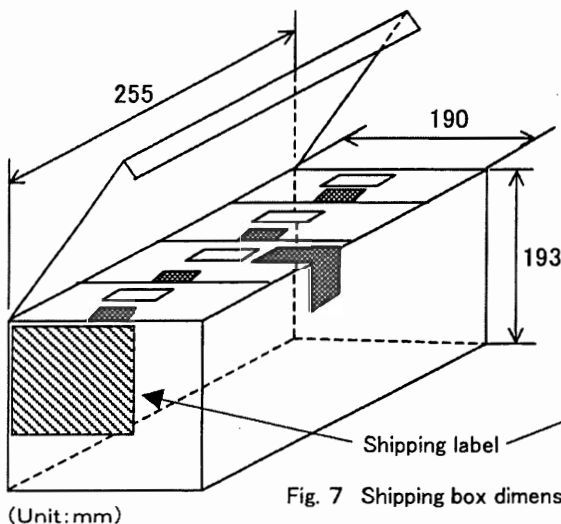
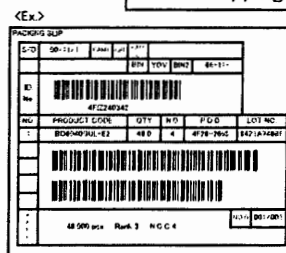


Fig. 7 Shipping box dimensions and shipping style

2. 7. Packing materials

| Item | Material |
|-----------------------|-----------|
| Embossed carrier tape | PS |
| Cover tape | PET + PE |
| Reel | PS |
| Unit box | Cardboard |
| Shipping box | Cardboard |



2. 8. Others

2. 8. 1. Peelback strength

Cover tape peelback strength is 0.2~0.7N.

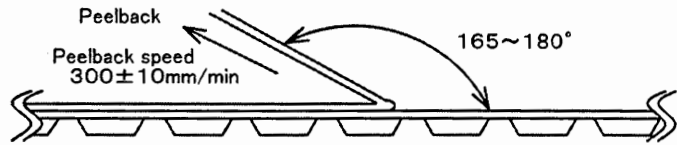


Fig. 8 Test method

2. 8. 2. Missing Ics

- (1) No consecutive dropouts.
- (2) A maximum 0.1% of specified number of products in each packing may be missing.

3. Storage conditions

3. 1. Storage environment

Recommended storage conditions are as follows :

- Temperature : 5~30°C
- Humidity : 40~70% RH

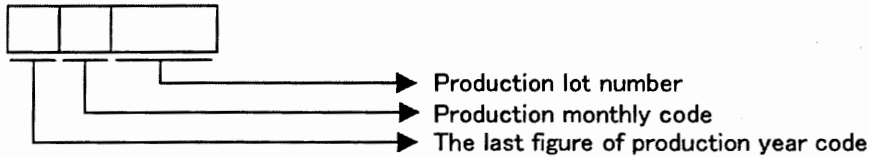
3. 2. Storage period

- Specified storage period : 1 year

3. 3. Specified storage period until soldering

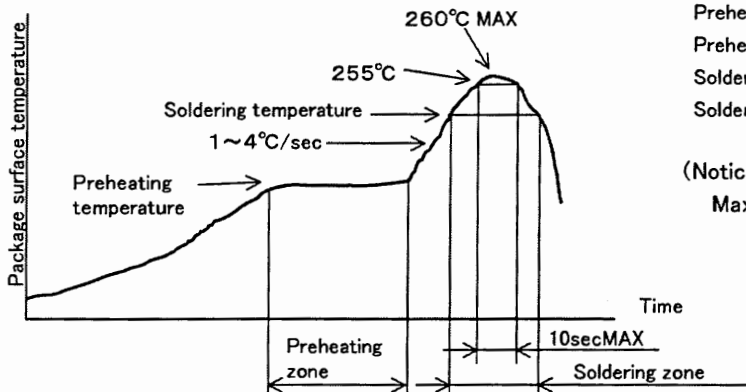
This package does not require additional drying treatment as long as the moisture condition at the mounting process is within our recommended mounting condition.

4. Marking lot number



5. Soldering conditions

5. 1. Recommended temperature profile for reflow



- Preheating temperature ; 130°C~190°C
- Preheating zone ; 120sec MAX
- Soldering temperature ; 220°C~230°C
- Soldering zone ; 60sec MAX

(Notice)
Maximum 2-times soldering

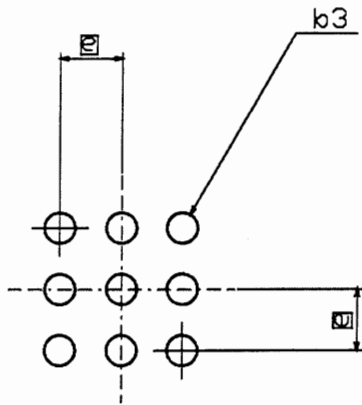
5. 2. About mounting with Sn-Pb solder paste.

Mounting with Sn-Pb solder paste is not recommended because it has a possibility of reducing reliability to connect with Sn-3.0Ag-0.5Cu solder balls.

5. 3. The wave soldering method is not supported.

5. 4. Partial heat supply method (by soldering iron) is not supported.

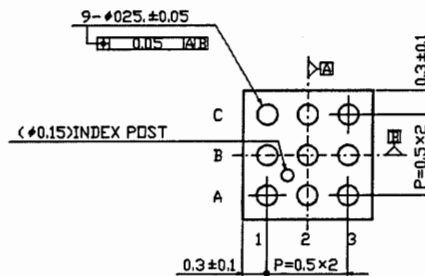
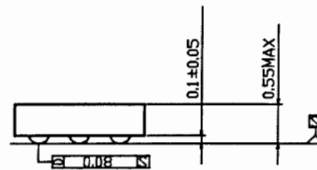
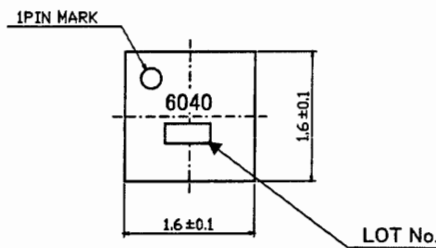
6. Footprint dimensions (Optimize footprint dimensions to the board design and soldering condition)



| Symbol | Reference Value |
|--------|-----------------|
| e | 0.50 |
| b3 | Φ0.25 |

(Unit: mm)

7. External dimensions



(Unit: mm)

8. Precautions

8. 1. Caution for handling

Silicon substrate surface is exposing to the side of this package.
Therefore, please pay careful attention to chip and crack, and handle without touching the side of package.

8. 2. Regarding the underfill material

In some case, the underfill material is applied in order to reinforce the solder junction of package.
Since there is a case that solder joint reliability may deteriorate according to the resin material or coating condition, please evaluate it sufficiently for its application.
In term of the coating condition, it is preferable that there is an enough material beyond the each four sides of package.

