

300mA High Maximum Absolute Ratings

LDO Regulator

BD35630HFV**●Description**

BD35630HFV is a LDO regulator with output current 300mA. The output accuracy is $\pm 1\%$ of output voltage. With external resistance, it is available to set the output voltage at random (from V_{FB} to 15.0V) and also is used for the wide applications of digital appliances. Over current protection (for protecting the IC destruction by output short circuit), circuit current ON/OFF switch (for setting the circuit current $0\mu A$ at shutdown mode), and thermal shutdown circuit (for protecting ICs from heat destruction by over load condition) are all built in.

●Features

- 1) Output current 300mA
- 2) High accuracy reference voltage circuit
- 3) Built-in Over Current Protection circuit (OCP)
- 4) Built-in Thermal Shut Down circuit (TSD)
- 5) With shut down switch
- 6) Output voltage variable type (V_{FB} to 15.0V)
- 6) Package : HVSO6

CONFIDENTIAL

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● Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	Vcc	24.0 * ¹	V
EN Voltage	VEN	24.0	V
Power Dissipation	HVSOF6 Pd	1700.0 * ²	mW
Operating Temperature Range	Topr	-10~+100	°C
Storage Temperature Range	Tstg	-55~+150	°C
Junction Temperature	TJmax	+150	°C

*1 Not to exceed Pd

*2 Reduced by 13.6mW for each increase in Ta of 1°C over 25°C.

(when mounted on a board 70.0mm x 70mm x 1.6mm Glass-epoxy PCB. (copper foil area : 2500mm²))

● Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Power Supply Voltage	Vcc	4.5	20.0	V
Output voltage	Vo	V _{FB}	15.0	V
EN Voltage	VEN	-	20.0	V
Output Current	Io	-	300	mA

★ This product should not be used in a radioactive environment.

● ELECTRICAL CHARACTERISTICS

BD35630HFV (Unless otherwise noted, Ta=25°C, EN=3V, Vcc=12V, R1=750kΩ, R2=82kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output Voltage 1	Vo1	7.920	8.000	8.080	V	Io=0mA
Output Voltage 2	Vo2	7.880	8.000	8.120	V	Tj=0 to 100°C Io=0mA→300mA
Circuit Current at shutdown mode	I _{sd}	-	0	5	μA	EN=0V, @OFF mode
Bias Current	I _{cc}	-	250	300	μA	
Output Current Ability	Io	300	-	-	mA	
Line Regulation	Reg.l	-	25	50	mV	Vcc=(Vo+1.8V)→15.0V, Io=300mA
Output Reference Voltage	V _{FB}	0.780	0.788	0.796	V	Io=0mA
EN Low Voltage	VEN (Low)	0	-	0.8	V	
EN High Voltage	VEN (High)	2.4	-	20.0	V	
EN Bias Current	I _{EN}	0.5	1.0	5.0	μA	

● Reference Data

BD35630HFV (Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{EN}=3\text{V}$, $V_{CC}=12\text{V}$, $R_1=750\text{k}\Omega$, $R_2=82\text{k}\Omega$)

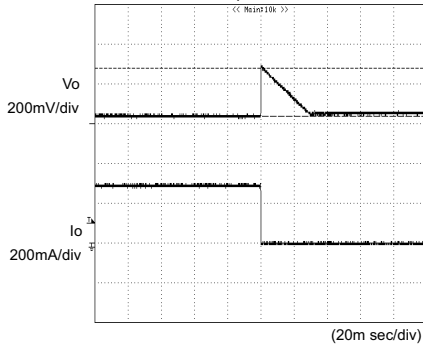


Fig.1 Transient Response
(300m→0mA), $C_o=1\mu\text{F}$

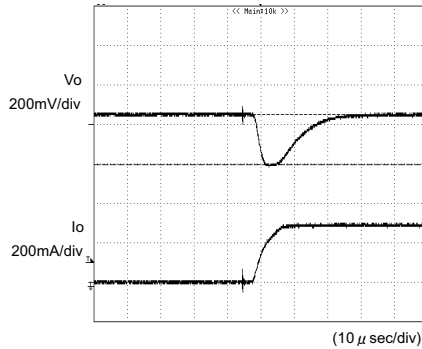


Fig.2 Transient Response
(0→300mA), $C_o=1\mu\text{F}$

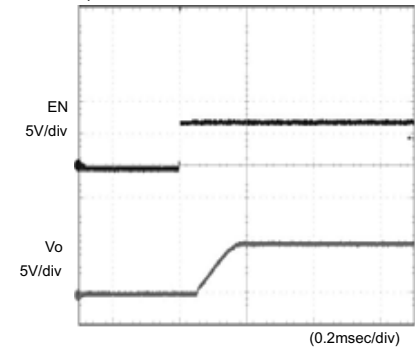


Fig.3 Waveform at output start
 $C_o=1\mu\text{F}$

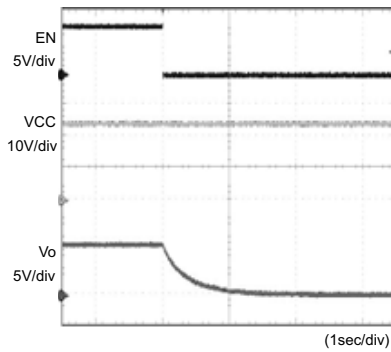


Fig.4 Waveform at output OFF
 $C_o=1\mu\text{F}$

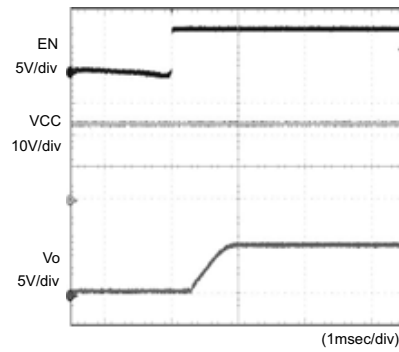


Fig.5 Input sequence 1
 $C_o=1\mu\text{F}$

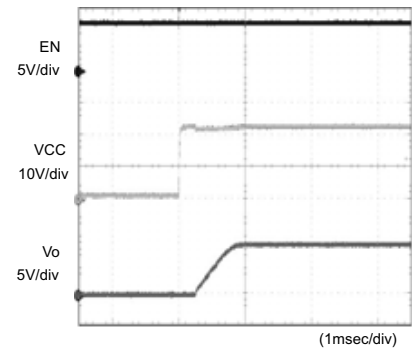


Fig.6 Input sequence 2
 $C_o=1\mu\text{F}$

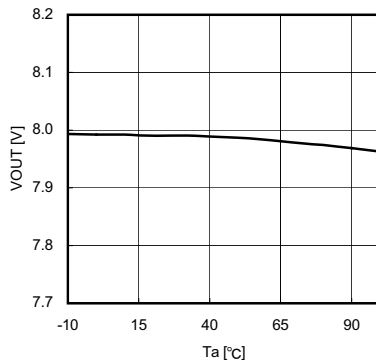


Fig.7 I_a - V_o ($I_o=0\text{mA}$)

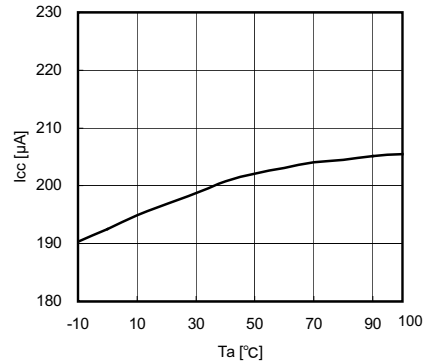


Fig.8 T_a - I_{cc}

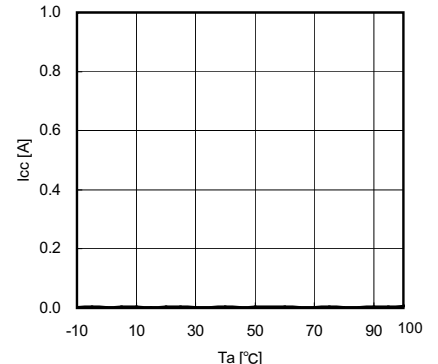


Fig.9 T_a - I_{cc}
($V_{CC}=12\text{V}$, $V_{EN}=0\text{V}$)

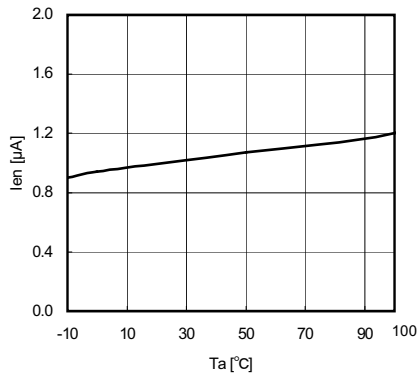


Fig.14 T_a - I_{EN}
($V_{CC}=12\text{V}$, $V_{EN}=3\text{V}$)

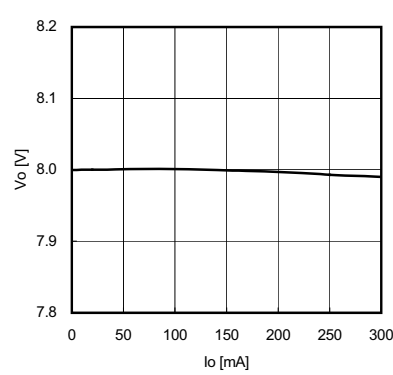


Fig.15 I_o - V_o

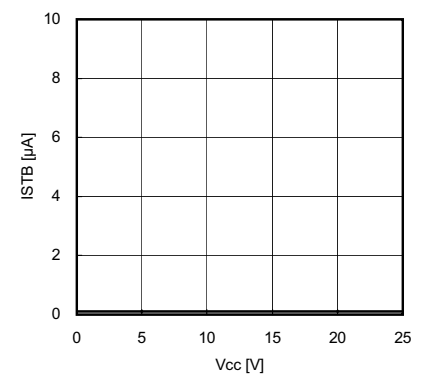


Fig.16 V_{CC} - I_{STB}
($V_{CC}=12\text{V}$, $V_{EN}=3\text{V}$)

●Reference Data (BD35630HFV)

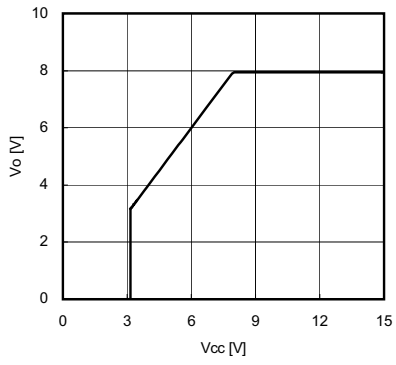
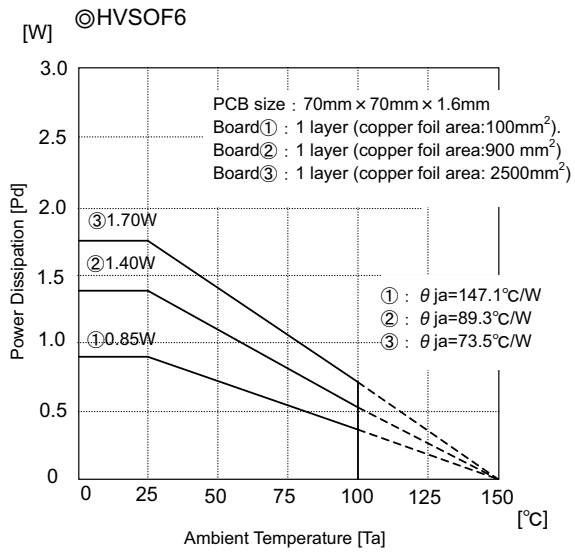
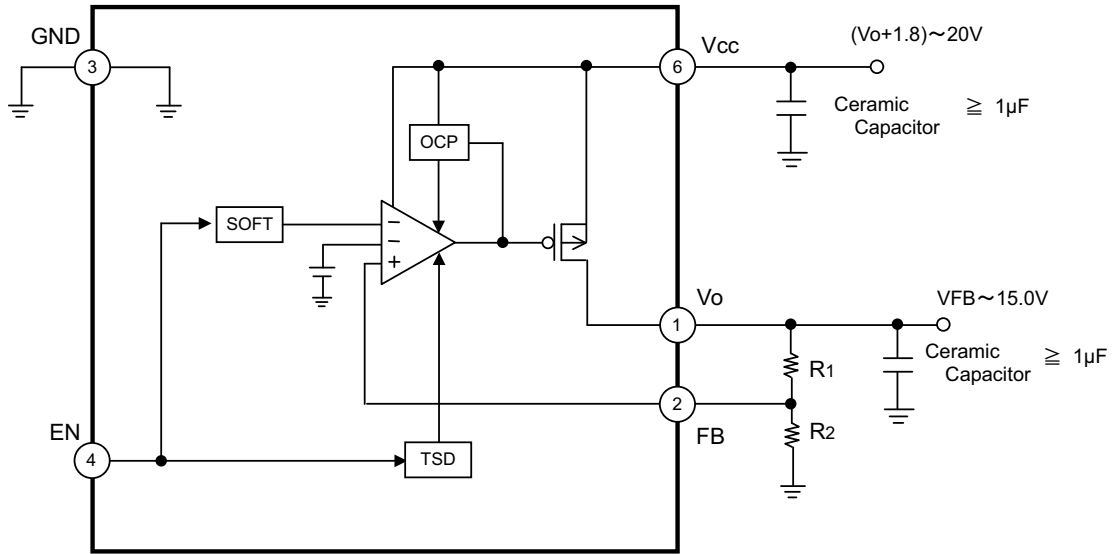


Fig.18 Vcc-Vo

●Heat Dissipation Characteristics



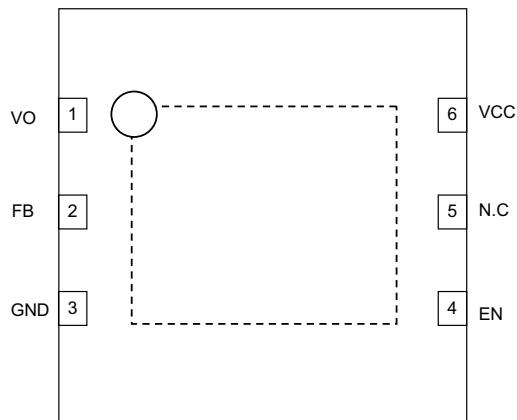
● Block Diagram
(HVSOF6)



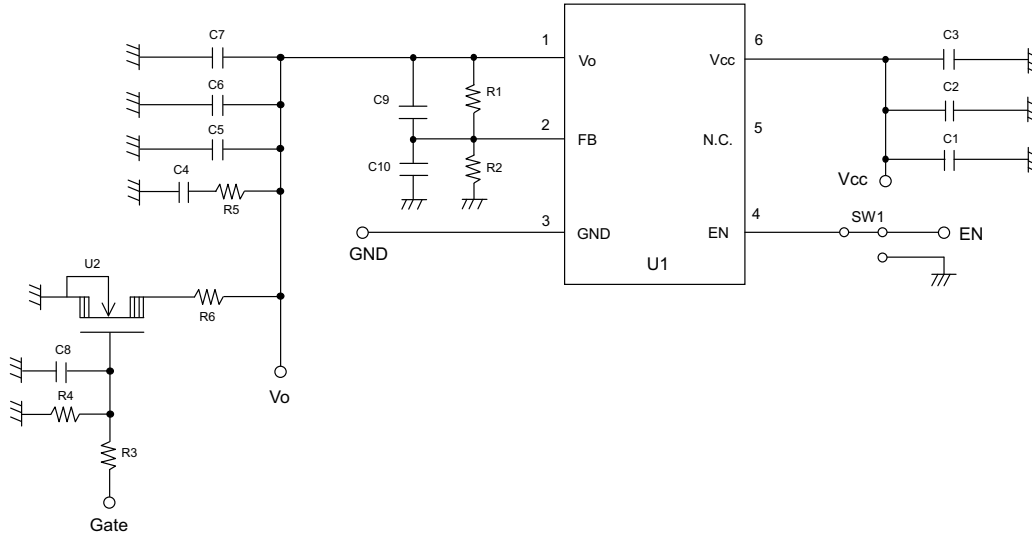
● Pin Function Table (HVSOF6)

Pin No.	Pin name	Pin Function
1	Vo	Output Voltage Pin
2	FB	Output Reference Voltage Pin (Feedback Pin)
3	GND	GND Pin
4	EN	Enable Pin
5	N.C	Open
6	Vcc	Input Voltage Pin

● Pin Layout (HVSOF6)



● Evaluation Board Circuit (HVSOF6)

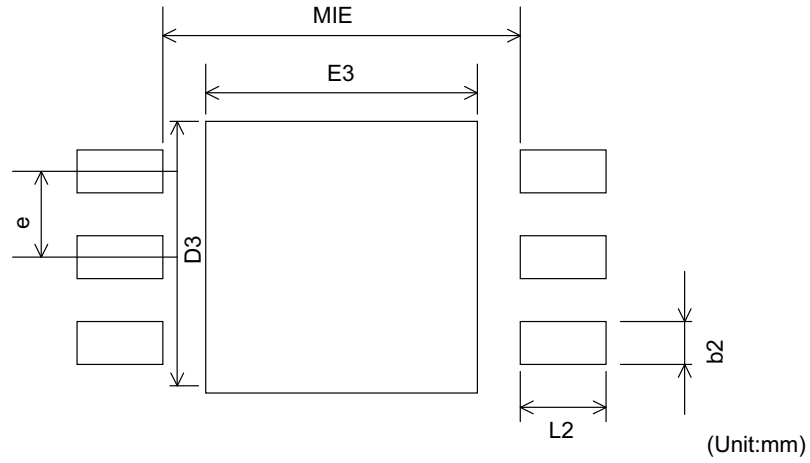


● Evaluation Board Parts List

Designation	Value	Part No.	Company
R1	750kΩ	MCR01PZPZF7503	ROHM
R2	82kΩ	MCR01PZPZF8202	ROHM
R3	-	-	-
R4	-	-	-
R5	-	-	-
R6	-	-	-
C1	1μF	CM105B105K16A	KYOCERA
C2	-	-	-
C3	-	-	-
C4	-	-	-
C5	1μF	CM105B105K16A	KYOCERA
C6	-	-	-
C7	-	-	-
C8	-	-	-
C9	-	-	-
C10	-	-	-
U1	-	BD35630HFV	ROHM
U2	-	-	-

●Reference landing pattern

◎HVSOF6



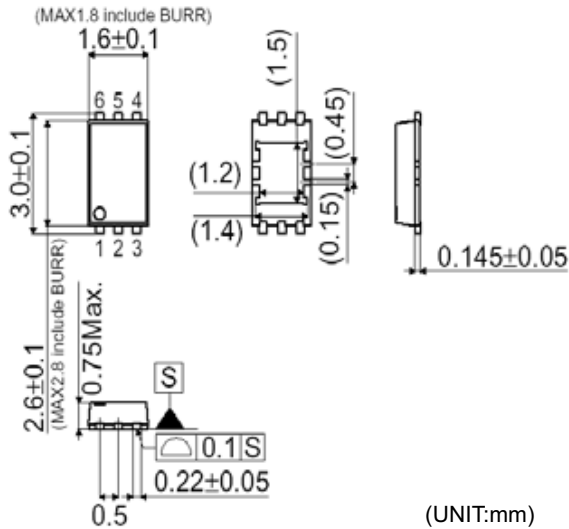
Lead pitch e	landing pitch MIE	landing length l2	landing pitch b2
0.50	3.00	0.55	0.25

central pad length D3	central pad pitch E3
1.60	2.60

*It is recommended to design suitable for the actual application.

●Dimension

◎HVSOF6



HVSOF6

● Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD35630HFV	175	15

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

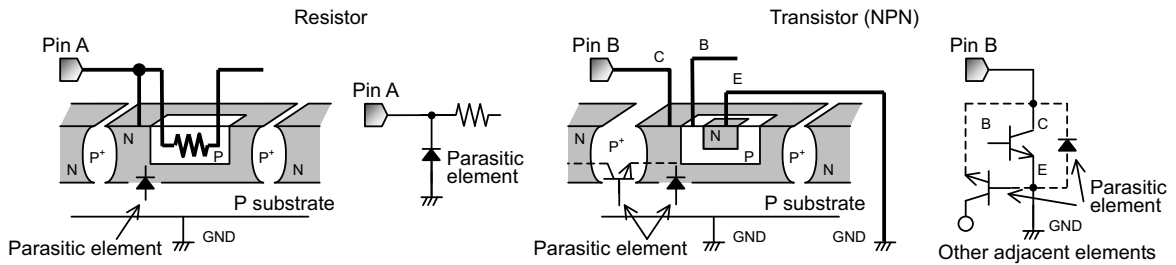
11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

