

Automotive Body Power Management LSI

LDO

Regulator

BD357XFP/HFP SERIES



TENTATIVE
ROHM CO.,LTD

DESIGN
INFORMATION

●Description

BD357XFP/HFP SERIES regulators feature a high 50 V withstand-voltage and are suitable for use with onboard vehicle microcontrollers. They offer the output current of 500 mA while limiting the quiescent current to 30 μ A (TYP). With these devices, a ceramic capacitor can be selected at the output for stable operation, the output tolerance is within $\pm 2\%$ over the wide ambient temperature range (-40 to 125°C), and the short circuit protection is folded-type to minimize generation of heat during malfunction. These devices are developed to offer most robust power-supply design under the harsh automotive environment. The BD357XFP/HFP Series provide ideal solutions to lower the current consumption as well as to simplify the use with battery direct-coupled systems.

●Features

- 1) Ultra-low quiescent current: 30 μ A (TYP.)
- 2) Low-saturation voltage type P-channel DMOS output transistors
- 3) High output voltage precision: $\pm 2\%$ / I_{omax} = 500 mA
- 4) Low-ESR ceramic capacitors can be used as output capacitors.
- 5) V_{cc} power supply voltage = 50 V
- 6) Built-in overcurrent protection circuit and thermal shutdown circuit
- 7) TO252-3,5 / HRP-5 Package

●Applications

- Onboard vehicle devices (body-control, car stereos, satellite navigation systems, etc.)

●Product line

	BD3570FP/HFP	BD3571FP/HFP	BD3572FP/HFP	BD3573FP/HFP	BD3574FP/HFP	BD3575FP/HFP
Output voltage	3.3V	5.0 V	Variable	3.3V	5.0 V	Variable
SW function	—	—	—	○	○	○

Package FP:TO252-3,TO252-5
HFP:HRP5

●Absolute maximum ratings (T_a=25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	V _{cc}	50 ※1	V
Switch Supply voltage	V _{sw}	50 ※2	V
Output current	I _o	500	mA
Power dissipation	P _d	1.2 (TO252-3) ※3	W
		1.3 (TO252-5) ※4	
		1.6 (HRP5) ※5	
Operating temperature range	T _{opr}	-40 to +125	°C
Storage temperature range	T _{stg}	-55 to +150	°C
Maximum junction temperature	T _{jmax}	150	°C

※1 Not to exceed P_d and ASO.

※2 for ON/OFF SW Regulator only

※3 TO252-3: Reduced by 9.6 mW/°C over 25 °C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

※4 TO252-5: Reduced by 10.4 mW/°C over 25 °C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

※5 HRP-5: Reduced by 12.8 mW/°C over 25 °C, when mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm).

●Operating Conditions

Parameter		Symbol	Min.	Max.	Unit
Input voltage	BD3570,3572,3573,3575FP/HFP	Vcc	4.5 ※6	36.0	V
	BD3571,3574FP/HFP	Vcc	5.5 ※6	36.0	V
Output current		Io	—	500	mA
Variable Output Voltage Range		Vo	2.8	12	V

※6 Please consider that the Output voltage would be dropped (Dropout voltage) according to the output current.

●Electrical Characteristics (Unless otherwise specified, Ta=-40 to125°C, Vcc=13.2 V, SW=3V ※7, Vo settings is 5V ※8)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Shut Down Current ※7	Ishut	—	—	10	μA	SW=GND
Bias current	Ib	—	30	50	μA	Io=0mA
Output voltage	Vo	Vo×0.98	Vo	Vo×1.02	V	Io=200mA, Vo:Please refer to Product line.
ADJ Terminal voltage ※8	VADJ	1.235	1.260	1.285	V	Io=200mA
Output current	Io	0.5	—	—	A	
Dropout voltage	ΔVd	—	0.25	0.48	V	Vcc=4.75V,Io=200mA ※9
Ripple rejection	R.R.	45	55	—	dB	f=120Hz,ein=1Vrms,Io=100mA
Line Regulation	Reg.I	—	10	30	mV	VCCD※10≤Vcc≤25V Io = 0 mA
Load Regulation	Reg.L	—	20	40	mV	0mA≤Io≤200mA
Swith Threshold voltage H ※7	SWH	2.0	—	—	V	Io=0 mA
Swith Threshold voltage L ※7	SWL	—	—	0.5	V	Io=0 mA
Swith Bias current ※7	SWI	—	22	60	μA	SW=5V,Io=0mA

※7 BD3573,3574,3575FP/HFP only

※8 BD3572,3575FP/HFP only

※9 BD3571,3572,3574,3575FP/HFP only

※10 BD3570,3573FP/HFP :VCCD=5.5V

BD3571,3572,3574,3575FP/HFP :VCCD=6.5V

●Reference Data: BD3574HFP (Unless otherwise specified, $T_a=25^\circ\text{C}$)

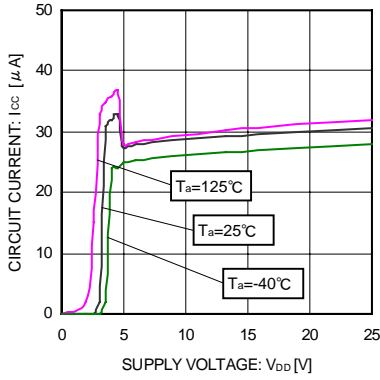


Fig. 1 Total Supply Current

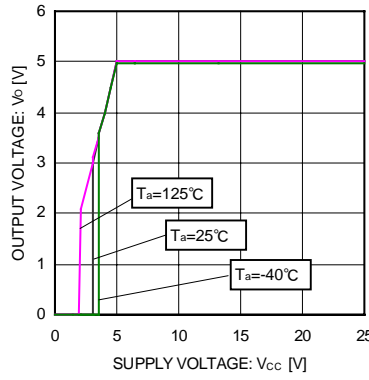


Fig. 2 Output Voltage VS Power Supply Voltage

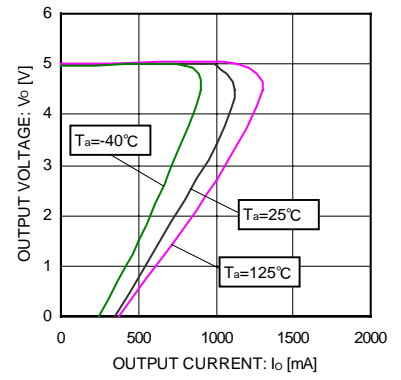


Fig. 3 Output Voltage VS Load

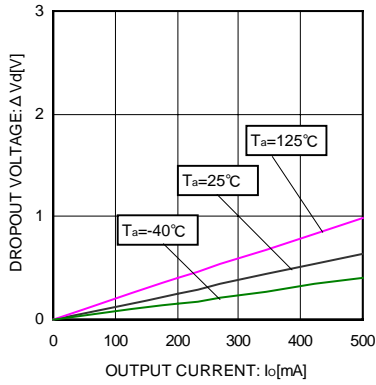


Fig. 4 Dropout Voltage

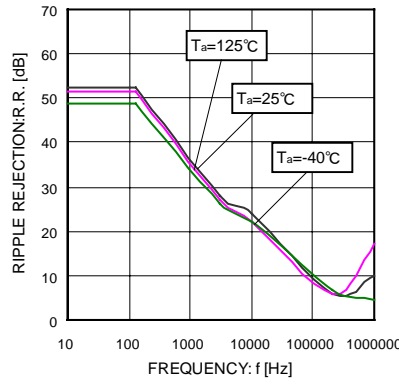


Fig. 5 Ripple rejection

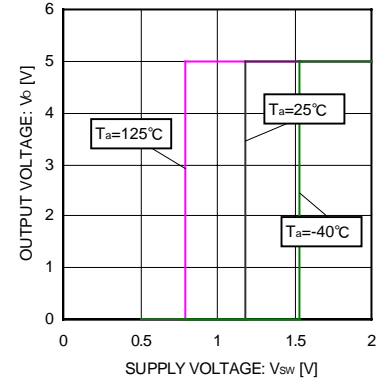


Fig. 6 Output Voltage VS SW Input Voltage

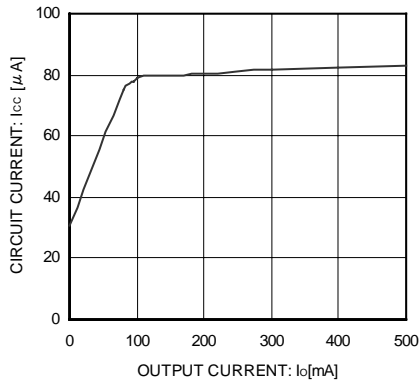


Fig. 7 Total Supply Current Classified by Load

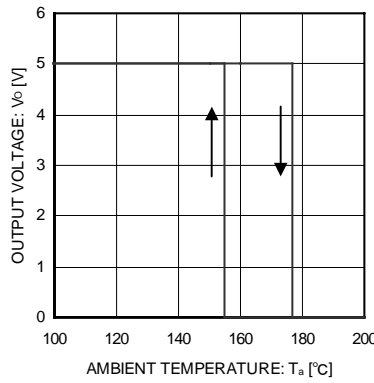


Fig. 8 Thermal Shutdown Circuit

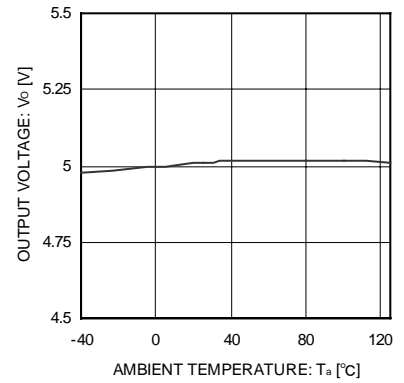


Fig. 9 Output Voltage VS Temperature

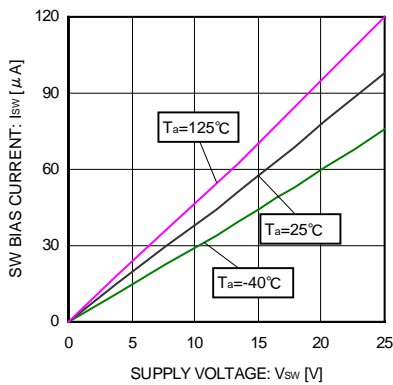


Fig. 10 SW Bias current

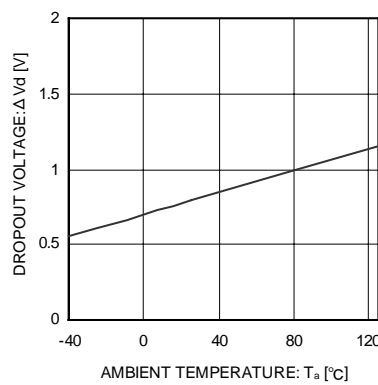


Fig. 11 Dropout voltage VS Temperature

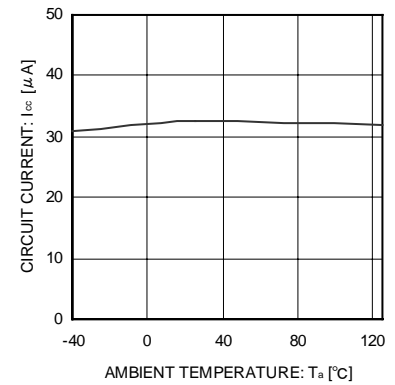


Fig. 12 Total Supply Current Temperature

●Block Diagram

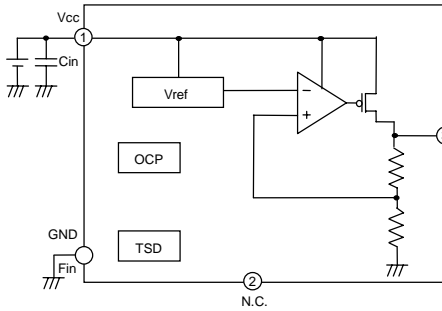


Fig.13 TO252-3

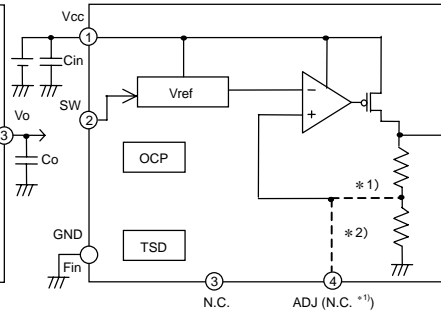


Fig.14 TO252-5

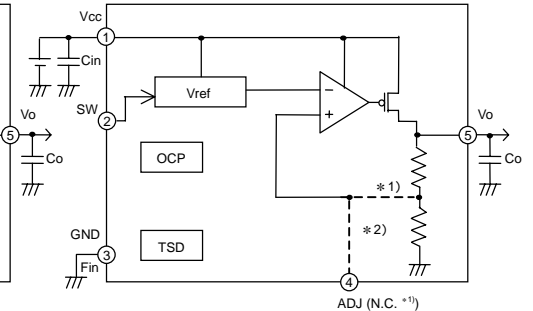


Fig.15 HRP-5

Cin : 0.33 μ F ~ 1000 μ F
Co : 0.1 μ F ~ 1000 μ F

* 1) For Fixed Voltage Regulator only
* 2) For adjustable Voltage Regulator only

●I/O Circuit diagram (All resistance values are typical.)

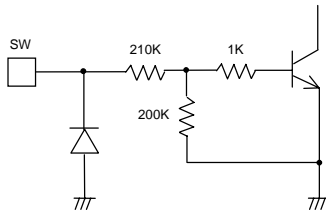


Fig.16 2PIN[SW]

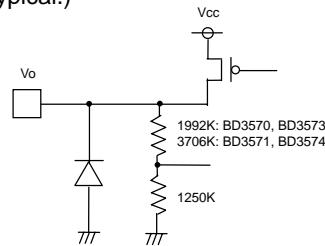


Fig.17 5PIN[Vo]
BD3570,3571,3573,3574

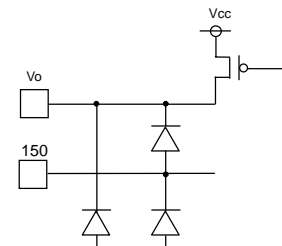
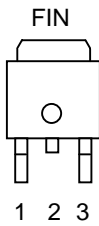


Fig.18 4.5PIN[ADJ,Vo]
BD3572,BD3575

●Pin Assignments

●TO252-3

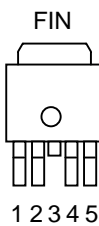


1 2 3

Fig. 19

Pin No.	Pin name	Function
1	Vcc	Power supply pin
2	N.C.	N.C. pin
3	Vo	Voltage output pin
Fin	GND	GND pin

●TO252-5

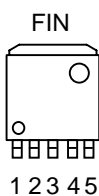


1 2 3 4 5

Fig.20

Pin No.	Pin name	Function
1	Vcc	Power supply pin
2	SW N.C.	Vo ON/OFF function pin N.C. pin(BD3572FP only)
3	N.C.	N.C. pin
4	N.C. ADJ	N.C. pin Output voltage setting pin(BD3572,3575FP only)
5	Vo	Voltage output pin
Fin	GND	GND pin

●HRP-5



1 2 3 4 5

Fig. 21

Pin No.	Pin name	Function
1	Vcc	Power supply pin
2	SW N.C.	Vo ON/OFF function pin (BD3573,3574,3575HFP only) N.C. pin
3	GND	GND pin
4	N.C. ADJ	N.C. pin Output voltage setting pin(BD3572,3575HFP only)
5	Vo	Voltage output pin
Fin	GND	GND pin

●Output Voltage Adjustment

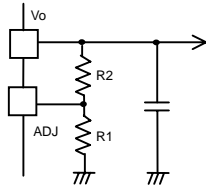


Fig.22

To set the output voltage insert pull-down resistor R1 between the ADJ and GND pins, and pull-up resistor R2 between the Vo and ADJ pins.

$$V_o = V_{ADJ} \times (R_1 + R_2) / R_1 [V]$$

{V_{ADJ}=1.26V(TYP.)}

The recommended connection resistor for the ADJ-GND is 30k~150kΩ.

●Setting of Heat

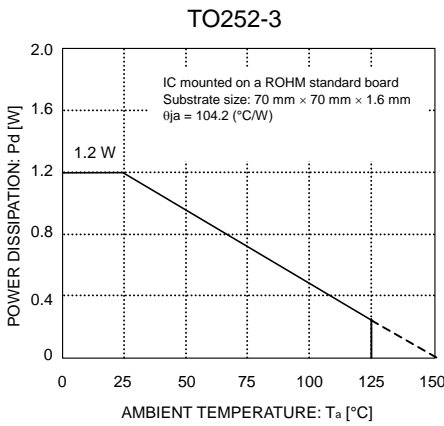


Fig. 23

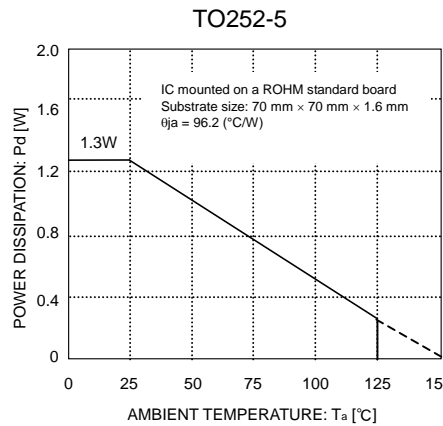


Fig. 24

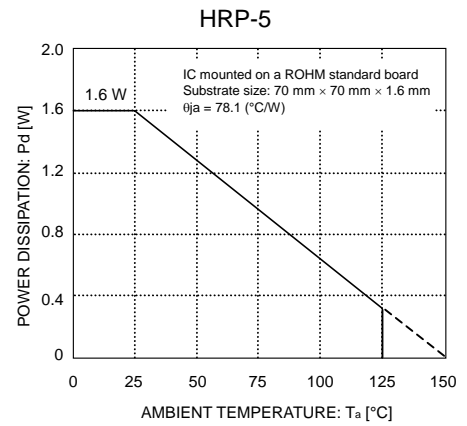


Fig. 25

Refer to the heat mitigation characteristics illustrated in Figs. 17 and 18 when using the IC in an environment where $T_a \geq 25^\circ\text{C}$. The characteristics of the IC are greatly influenced by the operating temperature. If the temperature is in excess of the maximum junction temperature T_{jmax} , the elements of the IC may be deteriorated or damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points, i.e., the protection of the IC from instantaneous damage and the maintenance of the reliability of the IC in long-time operation.

In order to protect the IC from thermal destruction, it is necessary to operate the IC not in excess of the maximum junction temperature T_{jmax} . Fig. 17 illustrates the power dissipation/heat mitigation characteristics for the TO252 package. Operate the IC within the power dissipation P_d . The following method is used to calculate the power consumption P_c (W).

$$P_c = (V_{CC} - V_o) \times I_o + V_{CC} \times I_{CC}$$

Power dissipation $P_d \leq P_c$

V_{CC} : Input voltage
 V_o : Output voltage
 I_o : Load current
 I_{CC} : Total supply current

The load current I_o is obtained to operate the IC within the power dissipation.

$$I_o \leq \frac{P_d - V_{CC} \times I_{CC}}{V_{CC} - V_o} \quad (\text{For more information about } I_{CC}, \text{ see page 12.})$$

The maximum load current I_{omax} for the applied voltage V_{CC} can be calculated during the thermal design process.

●Calculation example

Example: BD3571FP $V_{CC} = 12\text{ V}$ and $V_o = 5\text{ V}$ at $T_a = 85^\circ\text{C}$

$$I_o \leq \frac{0.624 - 12 \times I_{CC}}{12 - 5}$$

$$I_o \leq 89\text{mA} \quad (I_{CC} = 30\ \mu\text{A})$$

$\left(\begin{array}{l} \theta_{ja} = 104.2^\circ\text{C/W} \rightarrow 9.6\text{mAW}/^\circ\text{C} \\ 25^\circ\text{C} = 1.2\text{W} \rightarrow 85^\circ\text{C} = 0.624\text{W} \end{array} \right)$

Make a thermal calculation in consideration of the above so that the whole operating temperature range will be within the power dissipation.

The power consumption P_c of the IC in the event of shorting (i.e., if the V_o and GND pins are shorted) will be obtained from the following equation.

$$P_c = V_{CC} \times (I_{CC} + I_{short}) \quad I_{short} = \text{Short current}$$

●Peripheral Settings for Pins and Precautions

1) Vcc pins

Insert capacitors with a capacitance of $0.33\ \mu\text{F}$ to $1000\ \mu\text{F}$ between the Vcc and GND pins.
The capacitance varies with the application. Be sure to design the capacitance with a sufficient margin.

2) Capacitors for stopping oscillation for output pins

Capacitors for stopping oscillation must be placed between each output pin and the GND pin. Use a capacitor within a capacitance range between $0.1\ \mu\text{F}$ and $1000\ \mu\text{F}$. Since oscillation does not occur even for ESR values from $0.001\ \Omega$ to $100\ \Omega$, a ceramic capacitor can be used. Abrupt input voltage and load fluctuations can affect output voltages. Output capacitor capacitance values should be determined after sufficient testing of the actual application.

●Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (P_d) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Be sure to turn power off when mounting or dismantling jigs at the inspection stage. Furthermore, for countermeasures against static electricity, ground the equipment at the assembling stage and pay utmost attention at the time of transportation or storing the product.

7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junction is formed by the P layer and the N layer of each element, and a variety of parasitic elements will be constituted. For example, when a resistor and transistor are connected to pins as shown in Fig. 19,

- the P/N junction functions as a parasitic diode when $\text{GND} > \text{Pin A}$ for the resistor or $\text{GND} > \text{Pin B}$ for the transistor (NPN).
- Similarly, when $\text{GND} > \text{Pin B}$ for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins.

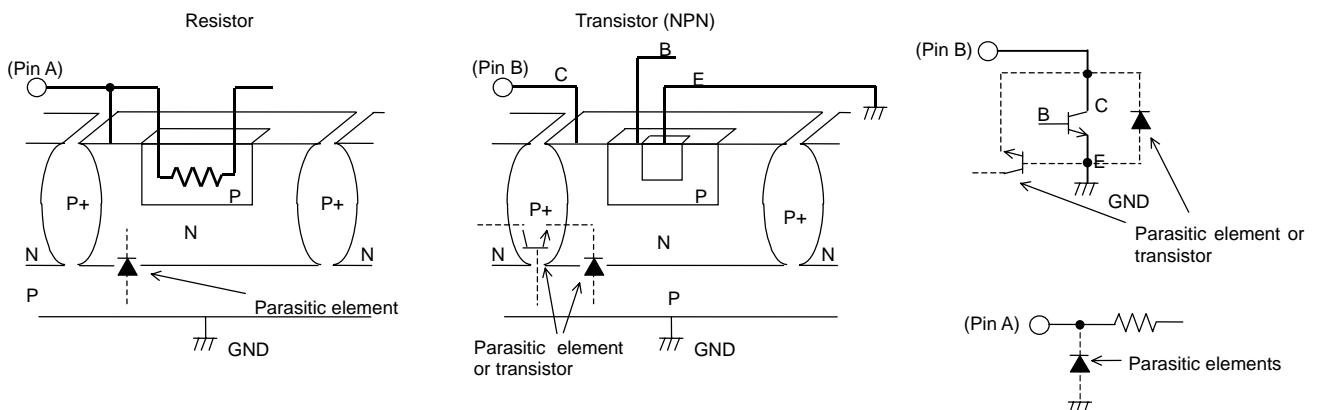


Fig. 26 Example of a Simple Monolithic IC Architecture

8) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) SW Pin

Do not apply the voltage to SW pin when the Vcc is not applied.
And when the Vcc is applied, the voltage of SW pin must not exceed Vcc.

10) Thermal shutdown circuit (TSD)

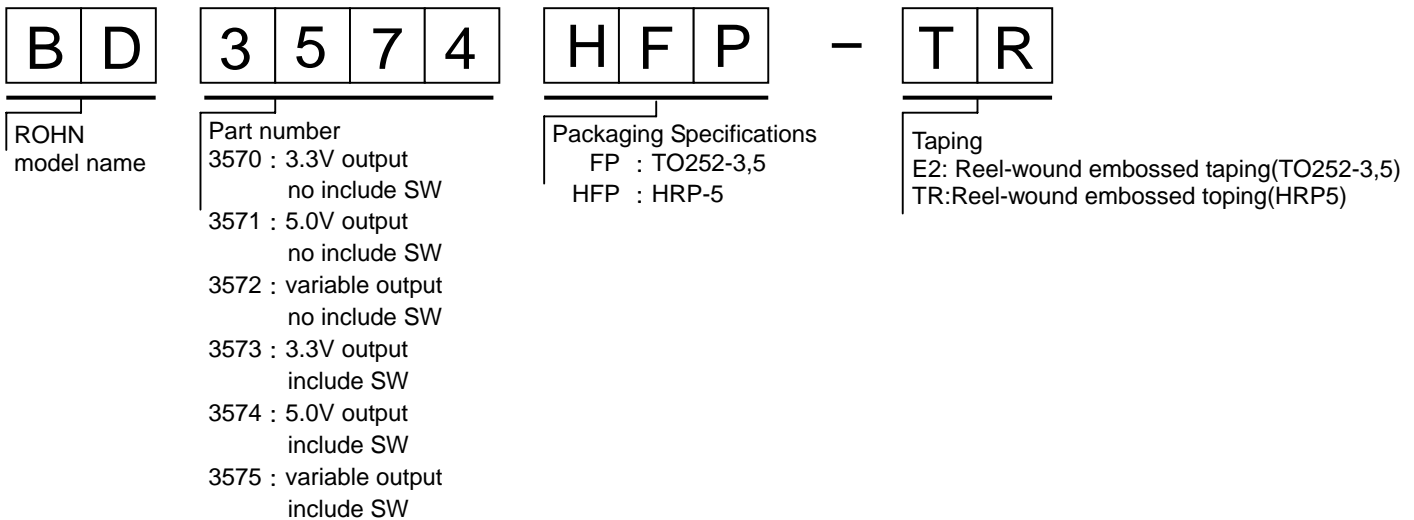
This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature T_j will trigger the thermal shutdown circuit to turn off all output power elements. The circuit automatically resets once the chip's temperature T_j drops.

The thermal shutdown circuit operates if the IC is under conditions in excess of the absolute maximum ratings. Never design sets on the premise of using the thermal shutdown circuit. (See Fig. 8)

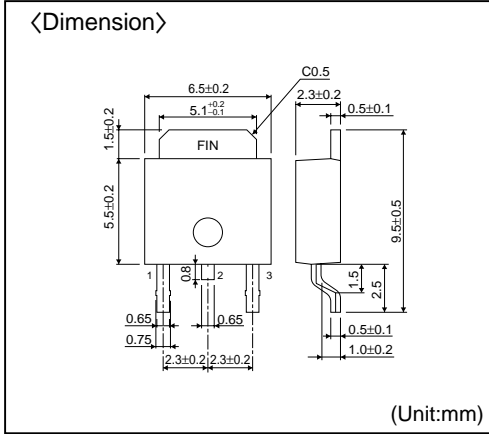
11) Overcurrent protection circuit (OCP)

The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures. (See Fig. 3)

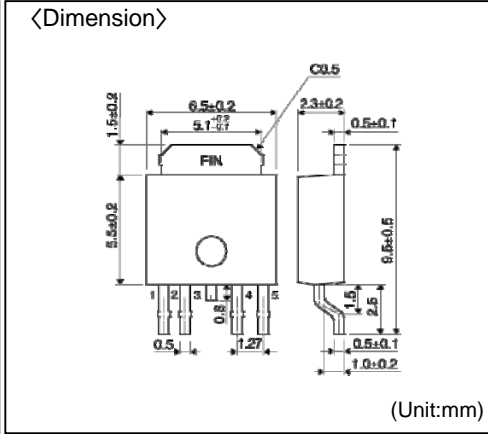
●Selecting a Model Name When Ordering



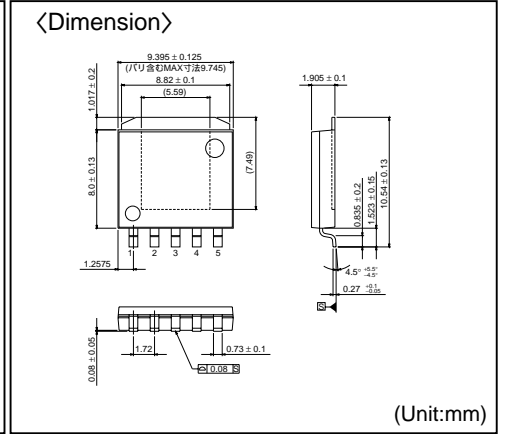
TO252-3



TO252-5

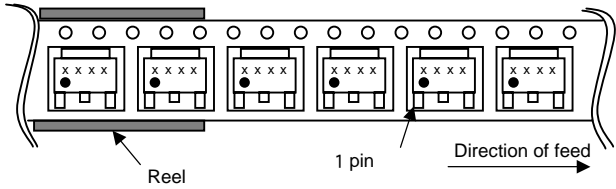


HRP-5



<Tape and Reel information > TO252-3,5

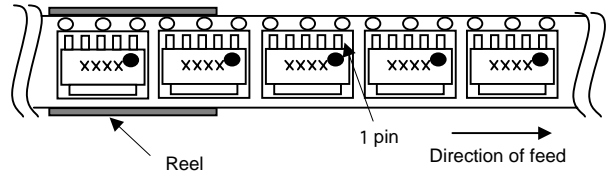
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1 pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

<Tape and Reel information>HRP5

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1 pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order, please order in times the amount of package quantity.